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Description

The invention relates to a digital transmission system having a transmitter and a receiver, the transmitter including a coder and the receiver including a decoder, for subband coding of a digital signal, such as a digital audio signal, having a given sampling rate F_S, the coder being responsive to the digital signal, for generating a number of M sub-band signals with sampling rate reduction, the coder dividing the digital signal band into successive subbands of band numbers m($1 \leqq m \leqq M$) increasing with frequency, the decoder being responsive to the M subband signals for constructing a replica of the digital signal, this decoder merging the subbands to the digital signal band, with sampling rate increase.

The invention also relates to a transmitter and a receiver for use in the transmission system, a coder for use in the transmitter, a decoder for use in the receiver, an analysis filter for use in the coder, a synthesis filter for use in the decoder, and a digital audio signal recording or reproducing apparatus comprising the transmitter and the receiver respectively.

A system for subband coding is known from the article entitled "The critical Band Coder - Digital encoding of speech signals based on the perceptual requirements of the auditory system" by M.E. Krasner, Proc. IEEE ICASSP80, Vol. 1, pp. 327-311, April 9-11, 1980. In this known system, use is made of a subdivision of the speech signal band into a number of subbands, whose bandwidths approximately correspond with the bandwidth of the critical bands of the human auditory system in the respective frequency ranges (compare fig. 2 in the article by Krasner). This subdivision has been chosen because on the basis of psycho acoustic experiments it may be expected that in a such like subband the quantization noise will be optimally masked by the signals within this subband when the quantizing takes account of the noise masking curve of the human auditory system (this curve indicates the threshold for masking the noise in a critical band by a single tone in the centre of the critical band, compare fig. 3 in Krasner's article.

The invention has for its object to provide a digital transmission system in which the information transmitted via the transmission medium between the transmitter and the receiver is divided in subbands having all approximately the same bandwidth, and which is constructed such that practically not distortion because of aliasing occurs in the reconstructed signal at the receiver side, and where the coder and decoder are very efficient with respect to computation time and complexity of the circuitry needed.

The digital transmission system in accordance with the with the invention is characterized in that the coder comprises analysis filter means and a signal processing unit, the analysis filter means comprises M analysis filters each having one input and two outputs, the 2 M outputs on the filters being coupled to 2 M outputs of the analysis filter means for supplying 2 M output signals with a sampling rate F_S/M, each analysis filter being adapted to apply two different filterings on the signal applied to its input and to supply each of the two different filtered versions of that input signal to a corresponding one of the two outputs, each one of the 2M filter outputs being coupled to a corresponding one of 2M inputs of a signal processing unit, the processing unit having M outputs coupled to M outputs of the coder for supplying the M subband signals, the signal processing unit being adapted to supply output signals on each of M outputs, an output signal being a combination of at least a number of input signals applied to its 2M inputs, the decoder comprises another signal processing unit and synthesis filter means, the other signal processing unit having M inputs for receiving the M subband signals and having 2 M outputs, the synthesis filter means comprising M synthesisfilters each having 2 inputs, and one output coupled to the decoder output, the other signal processing unit being adapted to generate an output signal on each of its 2 M outputs, an output signal being a combination of at least a number of input signals applied to its M inputs, each pair of outputs of the other signal processing unit being coupled to a pair of two inputs of a corresponding one of the M synthesis filters, each synthesis filter having one output, each synthesis filter being adapted to apply different filterings on the two signals applied to the two inputs and to supply a combination of the two filtered signals to its output, each output can be coupled to the output of the synthesis filter means for supplying the replica of the digital signal having a sampling rate F_S, in that the coder is adapted to divide the digital signal band into successive subbands having approximately equal bandwidths, and in that the coefficients of each of the analysis and synthesis filters are derived from the coefficients of a standard filter having a low pass filter characteristic with a bandwidth approximatly equal to half the bandwidth of the subbands, and that the coefficients for the analysis filters and the synthesis filters are derived from a standard filter having an odd number of coefficients, that M is an even number and that for making the number of coefficients of the standard filter equal to the number of multiplication factors of each of the analysis and synthesis filters, zeroes are added to the array of coefficients of the standard filter.

The measures according to the invention are based on the recognition that computation can be greatly simplified by arranging a sample rate decreaser in the form of the first unit before the analysis filters in the transmitter and by arranging a sample rate increaser in the form of the second unit behind the synthesis filters in the receiver, in that the computations are now applied on signals with a lower sampling rate.

Further, deriving the coefficients for the analysis filters and synthesis filters from a standard filter having an odd number of coefficients, results in a significant reduction in computations in the (other) processing units, in that there is a larger symmetry in the coefficients for the (other) processing unit.

It should be noted that the publication "Digital filtering by polyphase network: application to sample-rate alteration and filter banks" by M.G. Bellanger et al. in IEEE Trans. on ASSP, Vol. 24, No. 2, April 1976, pp. 109-114 discloses a system in which a digital signal is divided into a number of subbands by means of a number of filters, the said filters being preceded by a sample rate decreaser. Such a construction simplifies computation in the filters in that signal processing in these filters can be applied to signals having a decreased sampling rate.

The transmitter in the known system however does not generate subbands of substantially equal bandwidths, in that the lowest subband in the known system has a bandwidth of half the bandwidth of the other bandwidths. Moreover the filters and the processing unit in the known system differ from the filters and the processing unit in the system according to the invention in that the filters apply two different filterings on the signals applied to their apply two different filterings on the signals applied to their inputs instead of one, such as in the known system. This makes the content of the information transfer between the filters and the processing unit according to the invention twice of that in the known system. This makes it possible, by making use of a proper choice for the filter coefficients in the filters, as well as by choosing an appropriate construction of the processing units at the transmitter and the receiver side, to realize a reconstructed signal at the receiver side that is practically devoid of any distortion because of aliasing. Contrary to this, the reconstructed signal in the known system is always subject to aliasing distortion, even for the most optimal construction of the filters and the processing units.

It should further be noted that EP 190.796 Al discloses a coder comprising analysis filter means and a signal processing unit and a decoder comprising an other signal processing unit and synthesis filter means. The known coder and decoder differ from the coder and decoder claimed in that no information is given as to how to obtain the multiplication values for the analysis or synthesis filters in the case that M is even, and the number of coefficients in the standard filter is odd.

Various embodiments of the analysis and synthesis filters are possible.

In one embodiment the system on the transmitter side may be characterized in that each analysis filter comprises a series arrangement of delay sections having equal delay (T), the input of the filter being coupled to the input of the first delay section, outputs of at least a number of odd numbered delay sections in the series arrangement being coupled to corresponding inputs of a first signal combination unit, outputs of least a number of even numbered delay sections in the series arrangement being coupled to corresponding inputs of a second signal combination unit, outputs of the first and second signal combination unit being coupled to the first and second output respectively of the filter. Preferably, the outputs of odd numbered delay sections being coupled to inputs of the first signal combination unit only, and outputs of even numbered delay sections are coupled to inputs of the second signal combination unit only. In another embodiment, the system may be characterized in that each analysis filter comprises two series arrangements of delay sections having equal delay (2T), the input of the filter being coupled to the inputs of the first and at least a number of other delay sections in each series arrangement, the outputs of the two series arrangements being coupled to the first and second output of the filter respectively, a further delay section having a delay (T) that equals half the delay of the delay sections in the series arrangements, being coupled in the signal path from the input to the second output of the filter, the said further delay section not being included in the signal path from the inputto the first output of the filter.

One the receiver side, the system may be characterized in that each synthesis filter comprises two series arrangements of delay sections, having equal delay (2T), the first and second inputs of the filter being coupled to an input of the first delay section of the first and second series arrangement respectively, outputs of at least a number of delay sections in the first series arrangement being coupled to corresponding inputs of a signal combination unit, outputs of at least a number of delay sections in the second series arrangement also being coupled to corresponding inputs of the signal combination unit, an output of the signal combination unit being coupled to the filter output, a further delay section having a delay (T) that equals half the delay of the delay sections in the series arrangements, being coupled in the signal path from the second input to the output of the filter, the said further delay section not being included in the signal path from the first input to the output of the filter.

In another embodiment, the system may be characterized in that that each synthesis filter comprises a series arrangement of delay sections having equal delay (T), the first input of the filter being coupled to inputs of at least a number of odd numbered delay sections in the series arrangement, the second input of the filter being coupled to inputs of at least a number of even numbered delay sections in the series arrangement, the output of the last delay section being coupled to the output of the filter. Preferably, the first filter input is coupled to

inputs of odd numbered delay sections only, and the second filter input is coupled to inputs of even numbered delay sections only.

Also various embodiments of the signal processing unit in the transmitter and the other processing unit in the receiver are possible. In one embodiment the signal processing unit comprises M signal combination units, each having an output coupled to a corresponding one of the M outputs of the signal processing unit, in that for each signal combination unit, at least a number of inputs of the 2M inputs of the processing unit are coupled to corresponding inputs of the said signal combination unit, via corresponding multiplication units. The corresponding other signal processing unit on the receiver side then comprises 2M signal combination units, each having an output coupled to a corresponding one of the 2M outputs of the processing unit, in that, for each signal combination unit, at least a number of inputs of the M inputs of the processing units are coupled to corresponding inputs of the said signal combination unit, via corresponding multiplication units.

On the transmitter side the system may be further characterized in that the two outputs of each analysis filter are each coupled to their corresponding inputs of the signal processing unit via a corresponding signal amplification unit, both amplification units being adapted to amplify the signals applied to their inputs by the same complex value, the complex values preferably being different for amplification units coupled to different analysis filters. In addition each output of the processing unit may be coupled to its corresponding output of the coder via a series arrangement of a signal amplification unit and real value determinator, the signal amplification unit being adapted to amplify the signal applied to its input by a complex value.

On the receiver side, the system may be further characterized in that the two outputs of each pair of outputs of the other signal processing unit are each coupled to their corresponding input of a synthesis filter via a corresponding signal amplification unit, both amplification units being adapted to amplify the signals applied to their inputs by the same complex value, the complex values preferably being different for amplification units coupled to different synthesis filters.

In addition the M inputs of the decoder may be coupled to their corresponding one of the M inputs of the other processing unit via a signal amplification unit, the signal amplification unit being adapted to amplify the signal applied to its input by another complex value.

The invention will now be explained further with reference to a number of embodiments in the following figure description. The figure description discloses in

figure 1 an embodiment of the transmission system in accordance with the invention, in the form of a block diagram,

figure 2 the realization of the sample rate increase by means of the first unit,

figure 3 and 4 two embodiments of the analysis filter in the system,

figure 5 and 6 two embodiments of the synthesis filter in the system,

figure 7 an embodiment of the signal processing unit in the transmitter or the other signal processing unit in the receiver,

figure 8 another embodiment of the transmitter in the system,

figure 9 another embodiment of the receiver in the system,

figure 10 the derivation of the coefficients of the analysis filters in the receiver,

figure 11 another example of the processing unit in the transmitter, or the other signal processing unit in the receiver,

figure 12 a digital signal recording apparatus, and

figure 13 a digital signal reproduction apparatus.

Figure 1 discloses a block diagram of the digital transmission system. The system has an input terminal 1 coupled to an input 2 of a first unit 3, for receiving a digital system IN having a given sampling rate F_S. The first unit has M outputs 4.1 to 4.M on which ouput signals U_1 to U_M are available. The first unit 3 is adapted to realize a sample rate decrease by a factor M on the input signal IN applied to its input 2. The functioning of the first unit 3 will be explained later with reference to figure 2. M analysis filters 6.1 to 6.M are present, each analysis filter m having an input 5.m coupled to a corresponding one (4.m) of the M outputs of the first unit 3. m runs from 1 to M. Each analysis filter 6.m has two outputs 7.ma and 7.mb. Each analysis filter (6.m) is adapted to apply two different filterings on the signal (U_m) applied to its input (5.m) and to supply each of the two different filtered versions of that input signal (U_m) to a corresponding on of the two outputs (7.ma and 7.mb). The construction and the functioning of the analysis filters will be explained later with reference to the figures 3, 4 and 10. Each one of the 2M filter outputs 7.1a, 7.1b, 7.2a, 7.2b, ..., 7.ma, 7.mb, ..., 7Ma, 7Mb are coupled to a corresponding one of 2M inputs 8.1, 8.2, ..., 8M, 8M+1, ..., 8.2M of a signal processing unit 9. The processing unit 9 has M outputs to 10.1 to 10.M. The processing unit 9 is adapted to supply different output signals on each of its M outputs, an output signal being a combination of at least a number of input signals applied to its 2M inputs.

The construction and functioning of the signal processing unit 9 will be explained later with reference to

the figures 7 and 8. If the outputs 10.1 to 10.M are identical to the M outputs of the filter means, then this means that the signal processing unit 9 supplies the M subband signals S_1 to S_M, each subband signal S_m being available on a corresponding one (10.m) of the M outputs of the processing unit 9.

The input signal IN applied to the input 1 and having a sampling rate of F_S, occupies a bandwidth equal to $F_S/2$. Division of the signal bandwidth by a factor of M this means that the bandwidth of the subbands B_1 to B_M all equal $F_S/2M$, see figure 10c, s_1 in figure 1 being a down sampled version of the signal present in subband B_1, s_2 being a down sampled version of the signal present in subband B_2, etc.

The M subband signals can, if necessary, further be processed, e.g. in an additional quantizer (not shown), in which an (adaptive) quantization can be applied on the signals in order to realise a significant reduction in bit rate. Examples of such quantizers can e.g. be found in the published European patent application No. 289.080.

The signal processing described above is carried out on the transmitter side of the transmission system. The transmitter in the system thus at least include the elements with reference numerals 3, 6.1 to 6.M and 9, and, if present, the quantizer.

The signals generated in the transmitter are supplied via a transmission medium, schematically indicated by reference numeral 11 in figure 1, to the receiver. This might make the application of a further channel coding of the signal necessary, in order to make an error correction possible at the receiver side. The transmission via the transmission medium 11 can be in the form of a wireless transmission, such as e.g. a radiobroadcast channel. However also other media are well possible. One could think of an optical transmission via optical fibres or optical discs, or a transmission via magnetic record carriers.

The information present in the M subbands can be transmitted in parallel via the transmission medium, such as is disclosed in figure 1, or can be transmitted serially. In that case time compression techniques are needed on the transmitter side to convert the parallel data stream into a serial data stream, and corresponding time expansion techniques are needed on the receiver side to reconvert the data stream into a parallel date stream, so that the M subband signals S_1 to S_M can be applied to respective ones of the M inputs 12.1 to 12.M of another processing unit 13. The processing unit 13 has 2M outputs 14.1 to 14.2M. The other signal processing unit 13 is adapted to generate an output signal on each of its 2M outputs, an output signal being a combination of at least a number of input signals applied to its M inputs.

The construction and functioning of the other signal processing unit 13 will be explained later with reference to the figures 7 and 9. Pairs of outputs, such as 14.1 and 14.2, of the other processing unit 13 are coupled to pairs of inputs, such as 15.1a and 15.1b, of a corresponding one of M synthesis filters 16.1 to 16.M. Each synthesis filter 16.m has one output 17.m. The synthesis filters are applied to apply different filterings on the two signals applied to their two inputs and to supply a combination of the two filtered signals to their output. The construction and functioning of a synthesis filter will be explained later with reference to the figures 5, 6 and 10. The output (17.m) of each synthesis filter (16.m) is coupled to a corresponding one (18.m) of M inputs 18.1 to 18.M of a second unit 19. An output 20 of the second unit is coupled to an output 21 of the transmission system. The functioning of the second unit 19 will be explained later with reference to figure 2.

The receiver in the system includes at least the elements with reference numerals 13, 17.1 to 17.M and 19.

If the subband signals have been quantized at the transmitter side, a corresponding dequantizer will be needed in the receiver. Such a dequantizer should be coupled before the other signal processing unit 13. Examples of such dequantizers can also be found in the previously mentioned European patent application No. 289.080. The signal processing at the receiver side need to be such that signals u_1 to u_m are present at the outputs of the synthesis filters 16.1 to 16.M, and that a reconstructed signal OUT is present at the output terminal 21 which, in the ideal case, equals the input signal IN, applied to the input terminal 1.

Figure 2 discloses the functioning of the first and second units 3 and 19 respectively. The signal IN applied to the input terminal 1 is given schematically in figure 2(a) as a function of time.

Figure 2a discloses the samples from which the input signal IN is built up. It discloses only the location of the samples in time, not the amplitude of the samples. The samples are located a time interval T_1, which equals $1/F_S$, apart. The sampling rate of the input signal thus equals F_S. In the example of figure 2, it is assumed that M equals 8. The signals given in figure 2b to 2i (again only the locations in time, not the amplitudes are given) disclose the signals U_8 to U_1 present at the outputs 4.1 to 4.8 respectively of the unit 3. The unit 3 acts in fact as a commutator in that it distributes the each time eight samples contained in consecutive imaginary blocks cyclically to the eight outputs, see also the commutator 3 in figure 8.

From figure 2 it is clear that the output signals available at the M outputs of the unit 3 have a sampling rate of F_S/M. The samples in the output signals are now spaced a time interval T, which equals $M.T_1$, apart.

The reconstruction of the output signal OUT in the second unit 19 will be explained hereafter. The unit 19 can also be considered to be a commutator, in that it cyclically couples each of the M inputs 18.1 to 18.8 with

the output 20. In this case, samples occur after each other at the inputs 18.1 to 18.M, in this order, and are applied to the output 20 by the commutator 19. This is shown more clearly by the commutator 19 in figure 9.

The first unit can also be built up in a different way, namely by making use of a delay line having tappings at the correct locations along the said delay line. These tappings are then coupled to inputs of decimators, that bring the sampling rate down to the correct value.

It is even possible to combine the first unit and the analysis filters, expecially by making use of the delay line in the first unit for (a part of) the delay line(s) in the analysis filters, which is well known in the art.

The same reasoning is in fact valid for the second unit 19.

In this case interpolators are needed in order to realise the sample rate increase.

Figure 3 discloses a first embodiment of an analysis filter 6.m. An input 30 of the analysis filter, which equals the input 5.m in figure 1, is coupled to a series arrangement 31 of delay sections, having equal delays T. Outputs of the odd numbered delay sections 32.1, 32.3, ..., 32.n are coupled to inputs of a first signal combination unit 33. Outputs of the even numbered delay sections 32.2, 32.4, ..., are coupled to inputs of a second signal combination unit 34. Outputs of the first and second combination units 33 and 34 form the first and second output 35.1 and 35.2 respectively of the analysis filter 6.m. They equal the outputs 7.mb and 7.ma, respectively in fig. 1. The input 30 of the filter 6.m is coupled to an input of the second signal combination unit 34 via a multiplication unit 36.1. This multiplication unit multiplies the signals (samples) applied to its input by a factor of a_{om}. The outputs of the odd numbered delay sections are coupled to the inputs of the signal combination unit 33 via multiplication units 36.2, 36.4, ..., 36.n-1 and 36.n+1. They multiply the signals (samples) applied to their respective units by respective factors of a_{1m}, a_{3m}, ..., a_{nm}. The outputs of the even numbered delay sections are coupled to the inputs of the signal combination unit 34 via multiplication units 36.3, 36.5, ..., 36.n. They multiply the signals (samples) applied to their respective inputs by respective factors of a_{2m}, a_{4m}, ... In a more general definition of the signal combination units, these multiplication units can be considered as being included in the signal combination units. In that case, the signal combination units not only realize a summation of the signals applied to their inputs, but they realize a weighted combination (summation) of these signals. It is evident that, in the case that a multiplication unit has a factor a_{im} that equals zero, the coupling from the delay section to the signal combination unit including the said multiplication unit is dispensed with. It is further evident that, in the case that the said multiplication unit has a factor a_{im} that equals one, the multiplication unit is dispensed with, so that the coupling is a direct coupling.

Figure 4 shows another embodiment for the analysis filter 6.m. Although the circuit construction of the filter in figure 4 is different from the circuit construction of the filter of figure 3, it can carry out the same functioning and the same filterings, when some conditions are met. The filter of figure 4 includes two series arrangement 40 and 41 of delay sections having equal delay (2T). The input 30 of the filter is coupled to inputs of the delay sections in the series arrangement 40 via multiplication units 42.1 to 42.p-1 respectively and with the output 35.2 of the filter via a multiplication unit 42.p. That means that the series arrangement 40 includes p-1 delay sections 44.1 to 44.p-1. The input 30 of the filter is further coupled to inputs of the delay sections in the series arrangement 41 via multiplication units 4.1 to 43.q-1, and further with the output 35.1 of the filter via a multiplication unit 43.q. That means that the series arrangement 41 includes q-1 delay sections 45.1 to 45.q-1. The multiplication units 42.1 to 42.p multiply their input signals by a factor b_{1m}, b_{2m}, ..., b_{pm} respectively. The multiplication units 43.1 to 43.q multiply their input signals by a factor c_{1m}, ..., c_{qm} respectively. Signal combination units 46.1 to 46.p-1 are coupled to the outputs of the delay sections 44.1 to 44.p-1 of the series arrangement 40. Signal combination units 47.1 to 47.q-1 are coupled to the outputs of the delay sections 45.1 to 45.q-1 of the series arrangement 41. The output of the combination unit 47.q-1 is coupled to the filter output 35.1 via an additional delay section 48 having a delay T that equals half the delays of the delay sections in the series arrangements. The delay section 48 could have been provided somewhere else in the signal path from the input 30 to the output 35.1, provided that this delay section is not included in the signal path from the input 30 to the output 35.2.

What has been said with reference to figure 3 in the case that a multiplication unit has a multiplication factor that equals one or zero, is of course also valid in this case. In the latter case, let us assume that b_{2m} would be zero, this also means that the corresponding signal combination unit 46.1 that would otherwise have been coupled to the output of the relevant multiplication unit 42.2 can also be dispensed with. This means that the delay section 44.1 is directly connected to te delay section 44.2, or they can be combined into a delay section having a delay of 4T.

Under certain conditions the filter of figure 4 functions the same and realizes the same filterings on the input signal, as the filter of figure 3. The conditions for this are:

$p=q=(n+1)/2$, $b_{pm}=a_{om}$, $c_{qm}=a_{1m}$, $b_{p-1.m}=a_{2m}$, $c_{q-1.m}=a_{3m}$, ..., $b_{1m}=a_{n-1.m}$ and $c_{1m}=a_{nm}$.

In this case, it is assumed that n is an odd number. If, however n is an even number, the number of couplings to the combination unit 34 in figure 3 is one larger than the number of couplings to the combination unit 33. In

that case the conditions are as follows:
$q=p-1=n/2$, $b_{pm}=a_{om}$, $c_{qm}=a_{1m}$, $b_{p-1.m}=a_{2m}$, $c_{q-1.m}=a_{3m}$, ..., $b_{1m}=a_{nm}$ and $c_{1m}=a_{n-1.m}$.
Please note that the coupling including the multiplication unit 36.n+1 in the filter of figure 3, where n is even, is a coupling from the output of the series arrangement 31 to the signal combination unit 34!

Figure 5 shows a synthesis filter 16.m having two inputs 50.1 and 50.2 and one output 51. The inputs equal the inputs 15 ma and 15.mb and the output equals the output 17.m in fig. 1.
The synthesis filter includes two series arrangements 52 and 53 of delay sections having equal delay 2T. The filter 16.m further includes a signal combination unit 54 and an additional delay section 55 having a delay T that equals half the delay of the delay sections in the arrangements. The inputs 50.1 and 50.2 are coupled to inputs of the signal combination unit 54 via multiplication units 56.1 and 57.1 respectively. The series arrangement 52 includes p-1 delay sections 58.1 to 58 p-1. Outputs of these delay sections are coupled to corresponding inputs of the combination unit 54 via corresponding multiplication units 56.2 to 56.p. The multiplication units 56.1 to 56.p multiply their input signals by a factor of d_{1m} to d_{pm} respectively. The series arrangement 53 includes q-1 delay sections 59.1 to 59.q-1. Outputs of these delay sections are coupled to corresponding inputs of the combination unit 54 via corresponding multiplication units 57.2 to 57.q. The multiplication units 57.1 to 57.q multiply their input signals by a factor of e_{1m} to e_{qm} respectively. The output 60 of the combination unit 54 is coupled to the filter output 51. The delay section 55 is included between the input 50.2 and the input of the series arrangement 53. More generally, the delay section 55 can be included somewhere in the signal path from the input 50.2 to the output 51 such that it is not included in the signal path from the input 50.1 to the output 51.

For the filter 16.m to apply the correct filterings at the receiver side on the two signals applied to the inputs 50.1 and 50.2, when the m-th filter on the transmitter side is the filter 6.m of figure 3, the following condition should be met:
$p=q=(n+1)/2$, $d_{1m}=a_{om}$, $e_{1m}=a_{1m}$, $d_{2m}=a_{2m}$, $e_{2m}=a_{3m}$, ..., $d_{pm}=a_{n-1.m}$ and $e_{qm}=a_{nm}$. Again it is assumed that n is an odd number. In the same way as explained previously it can be found that for n is an even number, the conditions are as follows:
$q=p-1=n/2$, $d_{1m}=a_{1m}$, $e_{1m}=a_{1m}$, $d_{2m}=a_{2m}$, $e_{2m}=a_{3m}$, ..., $e_{qm}=a_{n-1.m}$ and $d_{pm}=a_{n.m}$.

Figure 6 shows another embodiment of the synthesis filter 16.m, denoted by 16.m'. The filter includes a series arrangement 65 of delay sections 66.1 to 66.n, having equal delay T. The input 50.1 is coupled to inputs of even numbered delay sections, via multiplication units 67.2, 67.4, ..., 67.n+1. n is thus considered to be an odd number. The input 50.2 is coupled to inputs of odd numbered delay sections via multiplication units 67.1, 67.3, ..., 67.n. In order for the filter 16.m' to carry out the correct filterings at the receiver side on the signals applied to the inputs 50.1 to 50.2, when the m-th filter on the transmitter side is the filter 6m of figure 3, the coefficients with which the multiplication units 67.1 to 67.n+1 multiply their input signals, should be as given in figure 6. These coefficients thus equal a_{nm}, $a_{n-1.m}$, ..., a_{2m}, a_{1m}, a_{om} respectively.

The choice for the coefficients a_{om} to a_{nm} for the filter 6.m of figure 3 will be further explained with reference to figure 10.

Figure 10(c) shows the the filterband of the digital signal, which is $F_S/2$ Hz broad. The total filterband is divided into M subbands B_1 to B_M of equal bandwidth $F_S/2M$. Figure 10(a) shows an imaginary or standard low pass filter having a filter characteristic of H(f) and a bandwidth F_B equal to half the bandwidth of the subbands. Figure 10(b) shows the impulse response of the low pass filter H(f) as a function of time. This impulse response is in the form of an array of impulses at equidistant time intervals $T_1=1/F_s$ spaced apart. The impulse response is characterized by an array of values h_0, h_1, h_2, ... indicating the amplitude of the impulses at the time intervals $t = 0, T_1, 2T_1, ...$

Figures 10(d) to (g) show how the multiplication factors for the multiplication units in the filters 6.1 to 6.M can be obtained using the impulse response of the standard low pass filter H(f). As can be seen the factors a_{01} to a_{oM}, being the multiplication factors for the multiplication units 36.1 in the filters 6.1 to 6.M, see Figure 3, equal h_0 to h_{M-1} respectively. The factors a_{11} to a_{1M}, being the multiplication factors for the multiplication units 36.2 in the filters 6.1 to 6.M, see Figure 3, equal h_M to h_{2M-1} respectively,the factors a_{21} to a_{2M} equal $-h_{2M}$ to $-h_{3M-1}$ respectively, the factors a_{31} to a_{3M} equal $-h_{3M}$ to $-h_{4M-1}$ respectively and so on, see especially the filter in Fig. 10d, which filter is worked out a little bit further. The standard filter H(f) has an odd number of impulses. This means that the filter has an odd number of coefficients h_0, h_1, h_2, ... The advantage of this will be made clear later.

Figure 7 shows an embodiment of the processing unit 9. The processing unit 9 includes X signal combination units 70.1 to 70.X. Y inputs, 71.1 to 71.Y, of the signal processing unit 9 are coupled via corresponding multiplication units 72.11 to 72.1Y to corresponding inputs of the combination unit 70.1. The Y inputs of the processing unit are also coupled to inputs of the combination unit 70.2, via corresponding multiplication units 72.21 to 72.2Y. This goes on for all the other combination units 70.x, where x runs from 1 to X inclusive. This

means that the y-th input 71.y is coupled to a corresponding input of the x-th combination unit 70.x via a corresponding multiplication unit 72.xy, where y runs from 1 to Y. It will be clear that Y equals 2M and the X equals M. The inputs 71.1 to 71.2M correspond in that order with the inputs 8.1 to 8.2M in figure 1. The outputs 74.1 to 74.M in that order correspond with the outputs 10.1 to 10.M in figure 1. The multiplication units 72.11 to 72.1Y, 72.21 to 72.2Y, 72.31 to 72.3Y, ... 72.X1 to 72.XY multiply their input signals by a factor of α_{11} to α_{1Y}, α_{21} to α_{2Y}, α_{31} to α_{3Y}, ... , α_{X1} to α_{XY} respectively. The factors α_{xy} can be calculated, using the following formula:

$$\alpha_{xy} = \begin{cases} \cos\varphi & \text{for y being an odd number} \\ \sin\varphi & \text{for y being an even number} \end{cases}$$

with $\varphi = (-1)^{x-1}\pi(x-1/2)\{1/2-(y-1)/DIV2/M\}$

As already said in the foregoing, the impulse response of the standard filter H(f) in figure 10b has an odd number of impulses, and thus an odd number of coefficients.

Figure 7 will also be used for explaining the construction and functioning of the other processing unit 13 on the receiver side. In that case, Y equals M and X equals 2M. In this case the inputs 71.1 to 71.M, in that order, correspond to the inputs 12.1 to 12.M in figure 1 and the outputs 74.1 to 74.2M, in that order, correspond to the outputs 14.1 to 14.2M in figure 1. The factors α_{xy} for the processing unit 13 can be calculated, using the following formula:

$$\alpha_{xy} = \begin{cases} \sin\varphi' & \text{for x being an odd number} \\ -\cos\varphi' & \text{for x being an even number} \end{cases}$$

with $\varphi'=(-1)^{y-1}\pi(y-1/2)\{1/2-(x-1)DIV2/M\}$

for an odd number of coefficients in the impulse response of H(f) in Fig. 10b.

By using these coefficients α_{xy} in the processing units on the transmitter and the receiver side, one realizes a transmission system that is practically fully devoid of any aliasing distortion. This in fact also requires bandwidth constraints imposed on the frequency transfer function of the standard filter. Preferably, the transition bandwidth of the said filter should not exceed Fs/4M. A numerical example is given in the table I for the coefficients for the processing unit 9 and in table II for the coefficients for the other processing unit 13, where M has been taken equal to 8, with the assumption that the impulse response H(f) in Fig. 10b has an odd number of coefficients. Table III includes the corresponding filter coefficients for the eight analysis filters 6.m. The coefficients for the corresponding synthesis filters 16.m can be derived from the coefficients in table III, in the way as explained with reference to Figures 5 and 6. Further the tables IV and V give the coefficients α_{xy} for the processing unit 9 and the other processing unit 13 and the table VI the coefficients a for the eight analysis filters 6.m, in the case that those coefficients would have been derived from the impulse response of a standard filter H(f) including an even number of coefficients. From table I and II, for the situation where the standard filter has an odd number of coefficients, it is clear that there is a large symmetry in the coefficients for the processing units. A large number of coefficients in one table is equal to each other, or differ only by its sign. This makes a large reduction in multiplying capacity possible. This contrary to the tables IV and V, for the situation where the standard filter has an even number of coefficients. Here the coefficients differ much more from each other.

As already explained, table III includes the filter coefficients derived from a standard filter having an odd number of impulses in the impulse response function. This is a filter that generates 127 impulses upon application of one input impulse, and which filter includes 127 filter-coefficients. The table however includes 128 coefficients. This has been realized by adding one zero as the first coefficient h_0, see the value for α_{01} in table III. Table VI has been obtained from a standard filter having an even number of (128) coefficients. In both cases, the impulse response of the standard filter are symmetrical. That means that two coefficients lying symmetrically around the middle are equal, except for their signs. This middle is for the odd numbered case at the location in time of the impulse h_{64}. This means that $h_1(=\alpha_{0.2})$ equals h_{127} $(=\alpha_{16.8})$, $h_2(=\alpha_{0.3})$ equals h_{126} $(\alpha_{16.7})$, h_3 $(=\alpha_{0.4})$ equals h_{125} $(=\alpha_{16.6})$, h_4 $(=\alpha_{0.5})$equals h_{124} $(=\alpha_{16.5})$, h_5 $(=\alpha_{0.6})$ equals h_{123} $(=\alpha_{16.4})$, h_6 $(=\alpha_{0.7})$ equals h_{122} $(=\alpha_{16.3})$, h_7 $(=\alpha_{0.8})$ equals h_{121} $(=\alpha_{16.2})$, h_8 $(=\alpha_{1.1})$ equals h_{120} $(=\alpha_{16.1})$, h_9 $(=\alpha_{1.2})$ equals h_{119} $(=\alpha_{15.8})$ and so on. All equalities except for their signs. h_{64}, which is $\alpha_{8.1}$, stands alone, see for this table III. The middle for the even numbered case is at a location exactly halfway between h_{63} and h_{64}.

This means that h_0 $(=\alpha_{0.1})$ equals h_{127} $(=\alpha_{16.8})$, h_1 $(=\alpha_{0.2})$ equals h_{126} $(=\alpha_{16.7})$, h_2 $(=\alpha_{0.3})$, equals h_{125} $(=\alpha_{16.6})$, h_3

($=\alpha_{0.4}$) equals h_{124} ($=\alpha_{16.5}$), h_4 ($=\alpha_{0.5}$) equals h_{123} ($=\alpha_{16.4}$), h_5 ($=\alpha_{0.6}$) equals h_{122} ($=\alpha_{16.3}$), h_6 ($=\alpha_{0.7}$) equals h_{121} ($=\alpha_{16.2}$), h_7 ($=\alpha_{0.8}$) equals h_{120} ($=\alpha_{16.1}$), h_8 ($=\alpha_{1.1}$), equals h_{119} ($=\alpha_{15.8}$), ... and so on ... until h_{63} ($=\alpha_{7.8}$) equals h_{64} ($=\alpha_{8.1}$).

All equalities except for their signs.

If there is a greater discrepancy than one, as explained above for the standard filter with an odd number of coefficients, between the number of coefficients in the standard filter and the coefficients α needed for the analysis (and synthetis) filters, then zeros should be added symmetrically starting from the outside and going to the inside.

Figure 8 shows an embodiment of the transmitter, which divides the input signal into eight subband signals. The output 7.1a and 7.1b of the analysis filter 6.1 are coupled to inputs of a corresponding amplification unit 80.1 and 81.1 respectively. The amplification units 80.1 and 81.1 amplify their input signals with a complex factor k_1 that is the same for both units 80.1 and 81.1. The outputs of these units 80.1 and 81.1 are coupled to inputs 85.1 and 85.9 respectively of a processing unit 82. The outputs 7.2a and 7.2b of the filter 6.2 are coupled to inputs of a corresponding amplification unit 80.2 and 81.2 respectively. They both amplify their input signals with a complex factor k_2. The outputs of these units are coupled to inputs 85.2 and 85.10 of the processing unit 82. In the same way, all the other filter outputs are coupled via corresponding amplification units 80.3, 81.3, ..., 80.8, 81.8 to inputs 85.3, 85.11,85.4, 85.12, ..., 85.8, 85.16 of the processing unit 82. Amplification units coupled to outputs of the same filter 6.m multiplying their input signals with the same complex value k_m. The complex values k_m equal the following formula:

$$k_m = \exp[j(m - 1)\pi/2M]$$

The processing unit 82 carries out a 2M(=16) point IFFT (Inverse Fast Fourier Transform) on the sixteen input signals applied to the inputs 85.1 to 85.16. The construction of such a processing unit is generally known from textbooks on digital signal processing, such as the book "Discrete-time signal processing: an introduction" by A.W.M. van den Enden and N.A.M. Verhoeckx, Prentice Hall, see especially Chapter 5.7, the pages 143-151. A 16-point IFFT has sixteen outputs. Only the first M(=8) outputs will be used. These outputs are generally associated with the low frequency outputs of block 82. These outputs 86.1 to 86.8 are each coupled via a corresponding amplification unit 83.1 to 83.8 respectively and a real value determining device 84.1 to 84.8 respectively to the terminals 10.1 to 10.8 respectively that are coupled to the transmission medium 11. The amplification units 83.1 to 83.8 amplify their input signals by a complex value V_1 to V_8 respectively. The complex value V_m equal the following formula:

$$V_m = \exp j\,\beta_m$$

Where β_m need to be chosen properly and should be chosen such that the behaviour of the circuit within the dashed block denoted by 9′ equals the behaviour of the circuit as described with reference to figure 7 and stable I or table IV. The advantage of the processing unit of figure 8 is that it can realize the functioning as explained with reference to figure 7 for an even as well as odd number of coefficients of H(f). In that case, only the values β_m need to be chosen differently. In general the complex values differ from each other for different values of m.

Figure 9 shows an embodiment of the receiver that can cooperate with the transmitter of figure 8. The terminals 12.1 to 12.8 are coupled to the first M(=8) inputs 92.1 to 92.8 respectively of a processing unit 91 via corresponding amplification units 90.1 to 90.8 respectively. These amplification units amplify their input signals by a factor of V_1' to V_8' respectively. The processing unit 91 carries out a 2M(=16) point FFT. Constructions of such units can also be found in the previously mentioned book of Van den Enden et al. Such units have 16 inputs. This means that a value of zero will be applied to the second M(=8) inputs 92.9 to 92.16 of the processing unit 91. Pairs of two outputs 93.1 and 93.9, 93.2 and 93.10, ..., 93.8 and 93.16 are coupled to the two inputs of corresponding filters 16.1, 16.2, ..., 16.8 via corresponding amplification units 94.1 and 95.1 respectively, 94.2 and 95.2 respectively, ..., 94.8 and 95.8 respectively. Amplification units 94.m and 95.m amplify their input signals by equal complex values of k_m'.

The complex values k_m' equal the following formula:

$$k_m' = \exp[-j(m - 1)/2M]$$

The complex values V_m' equal the following formula:

$$V_m' = (\exp(-j\,\beta_m')$$

where β_m' need to be chosen properly and should be chosen such that the behaviour of the circuit within the block 13′ indicated by dashed lines equals the behaviour of the circuit as described with reference to figure 7 and table II or table V. The advantage of the other processing unit of figure 9 is that it can also realize the functioning as explained with reference to figure 7 for an even as well as an odd number of coefficients for H(f). In that case, only the values β_m' need to be chosen differently.

Fig. 11 shows again another embodiment of the signal processing unit 9 of figure 1, denoted by 9″. The processing unit 9″ has switching means 100, and M signal combination units, of which only the first two are

shown and have the reference numberals 102 and 103, respectively. The inputs 8.1 to 8.2M of the processing unit 9″ are coupled to the 2M inputs of the switching means 100. These means 100 have one output 101 which is coupled to the inputs of all signal combination units. Only the couplings to the inputs 104 and 105 of the combination units 102 and 103 are given. The outputs of the M combination units are the outputs 10.1 to 10.M of the processing unit 9″. Each combination unit has a multiplication unit 106, a memory 107 having 2M storage locations, an adder 108 and an accumulating register 109.

The switching means 100 are adapted to arrange each time the samples in blocks of 2M samples that occur more or less at the same instant at the 2M inputs 8.1 to 8.2M, each sample at one input, in a serial fashion at the output 101. The contents of the memory 107 for the combination unit 102 and 103 are given in figure 11. The multiplication factors α_{11}, to $\alpha_{1.2M}$ and α_{21} to $\alpha_{2.2M}$ contained in the said memories equal the corresponding factors in the processing unit 9 in figure 7. The processing unit 9 and 9″ should of course carry out the same processing on the signals applied to their inputs. The memory 107 is controlled in such a way that it supplies the factor α_{11} to the input 111 of the multiplication unit 106, when the switching means 100 supply the sample that occurred at the input 8.1 to the input 112 of the unit 106. The contents of the register 109 is zero at this moment, so that after the multplication the result is stored in the register 109. Next, the sample that occurred at the input 82 is applied to the input 112 and the factor α_{12} is applied to the input 111 of the unit 106, and they are multiplied with each other.

By means of the adder 108, the result of this multiplication, that is applied to the input 113 of adder 108, is added to the contents of the register 109, that is applied to the input 114 of the adder 108, and stored in the register 109.

This processing continues for the multiplication with all the 2M factors contained in the memory 107. Moreover this processing is carried out in parallel in the other combination units, such as unit 103.

After the 2M-th multiplication, the result of this multiplication is added to the contents in the register. The contents then obtained is supplied to the output 10.1, by storing it in an additional buffer memory 110. Next, the contents of the register 109 is set to zero and a next cycle of 2M multiplications can begin. It is evident that the other processing unit 12 can be built up in the same way. Such processing unit comprises 2M signal combination units, such as the unit 102 in figure 11, will the difference that the memory 107 now contains M factors a_{11} to $\alpha_{1.M'}$ or α_{21} to $\alpha_{2.M}$ for the memory 107 in the unit 103. Further the switching means 100 are different, in that they have M inputs 12.1 to 12.M and that they arrange each time the samples in consecutive blocks of M samples that occur more or less at the same instant at the M inputs 12.1 to 12.M, each sample at one input, in a serial fash and the output 101. Further the register 109 is now set to zero after the M-th multiplication.

Figures. 12 and 13 show a transmission via magnetic record carriers. Figure 12 shows a digital signal recording apparatus, which includes the transmitter as shown in figure 1. The apparatus further includes recording means 120 having M inputs 121.1 to 121.M, each one coupled to a corresponding one of the M outputs of the signal processing unit 9. The apparatus is for recording a digital audiosignal to be applied to the input 1 on a magnetic record carrier 122 by means of at least one magnetic recording head 123.

The recording means 120 can be an RDAT type of recording means, which uses the helical scan recording principle to record the signal s_1 to s_M in slank tracks lying next to each other on the record carrier, in the form of a magnetic tape. In that case it might be necessary for the recording means 120 to incorporate means to realize a parallel-to-serial conversion on the signal applied to the inputs 121.1 to 121.M.

The recording means 120 can equally well be an SDAT type of recording means, in which the signals s_1 to s_m to be recorded are divided over a number of tracks, the said number of tracks not necessarily being equal to M, lying in parallel on, and in the length direction of the record carrier. Also in this case it might be necessary to realize parallel-to-serial conversion on the signals, e.g. if the number of tracks is less than M.

RDAT and SDAT type of recording means are well known in the art and can e.g. be found in the book "The art of digital audio" by J. Watkinson, Focal press, London, 1988. Therefore no further explanation is needed.

Figure 13 shows a digital reproduction apparatus, which includes the receiver as shown in figure 1. The apparatus further includes reproducing means 124 having M outputs 125.1 to 125.M, each one coupled to one of the inputs 12.1 to 12.M of the other signal processing unit 13.

The apparatus is for reproducing the digital signal, as it is recorded on the record carrier 122 by means of the apparatus of figure 12. Therefore the reproducing means 124 comprise at least one read head 126. The reproducing means can be an RDAT or SDAT type reproducing means. For a further explanation of the reproducing means in the form of an RDAt or SDAT type reproducing means, reference is made to the previously mentioned books of J. Watkinson.

It should be noted that the invention is not limited to the embodiments disclosed herein. The-invention equally applies to those embodiments which differ from the embodiments shown in respects which are not relevant to the invention. As an example, the present invention can be equally well applied in apparatuses such

as they are described in the Netherlands Patent applications 88.02.769 and 89.01.032, which both correspond to European patent application no 372601 and in which at least two signals are combined into a composite signal, are transmitted, and are split up in at least two signals at the receiver side.

Claims

1. A digital transmission system having a transmitter and a receiver, the transmitter including a coder (3,6,9) and the receiver including a decoder (13,16,19), for subband coding of a digital signal, such as a digital audio signal, having a given sampling rate F_S, the coder being responsive to the digital signal, for generating a number of M sub-band signals with sampling rate reduction, the coder dividing the digital signal band into successive subbands of band numbers m($1 \leqq m \leqq M$) increasing with frequency, the decoder being responsive to the M subband signals for constructing a replica of the digital signal, this decoder merging the subbands to the digital signal band, with sampling rate increase, wherein the coder (3,6,9) comprises analysis filter means (3,6) and a signal processing unit (9), the analysis filter means comprises M analysis filters (6.1 to 6.M) each having one input and two outputs, the 2 M outputs of the filters being coupled to 2 M outputs of the analysis filter means for supplying 2 M output signals with a sampling rate F_S/M, each analysis filter (6.1) being adapted to apply two different filterings on the signal applied to its input (5.1) and to supply each of the two different filtered versions of that input signal to a corresponding one of the two outputs (7.1a, 7.1b), each one of the 2M filter outputs being coupled to a correpsonding one of 2M inputs (8.1 to 8.2M) of a signal processing unit (9), the processing unit having M outputs (10.1 to 10.M) coupled to M outputs of the coder for supplying the M subband signals, the signal processing unit being adapted to supply output signals on each of M outputs, an output signal being a combination of at least a number of input signals applied to its 2M inputs, the decoder (13,16,19) comprises another signal processing unit (13) and synthesis filter means (16,19) the other signal processing unit having M inputs (12.1 to 12.M) for receiving the M subband signals and having 2 M outputs (14.1 to 14.2M), the synthesis filter means comprising M synthesisfilters (16.1 to 16.M) each having 2 inputs, and one output (20) coupled to the decoder output, the other signal processing unit (13) being adapted to generate an output signal on each of its 2 M outputs, an output signal being a combination of at least a number of input signals applied to its M inputs, each pair of outputs (14.1,14.2) of the other signal processing unit being coupled to a pair of two inputs (15.1a,15.1b) of a corresponding one of the M synthesis filters (16.1 to 16.M), each synthesis filter (16.1) having one output (17.1), each synthesis filter being adapted to apply different filterings on the two signals applied to the two inputs and to supply a combination of the two filtered signals to its output, each output can be coupled to the output of the synthesis filter means for supplying the replica of the digital signal having a sampling rate F_S, in that the coder is adapted to divide the digital signal band into successive subbands (B_1, B_2, ...) having approximately equal bandwidths, characterized in that the coefficients of each of the analysis and synthesis filters are derived from the coefficients of a standard filter (H(f)) having a low pass filter characteristic with a bandwith approximatly equal to half the bandwidth of the subbands, and that the coefficients for the analysis filters and the synthesis filters are derived from a standard filter having an odd number of coefficients, that M is an even number and that for making the number of coefficients of the standard filter equal to the number of multiplication factors of each of the analysis and synthesis filters, zeroes are added to the array of coefficients of the standard filter.

2. A digital transmission system as claimed in Claim 1, characterized in that the analysis filter means (3,6) comprises a first unit (3) having an input (2) coupled to the input (1) of the coder, for receiving the samples of the digital signal and M outputs (4.1 to 4.M) for supplying M output signals with a sampling rate of F_S/M, the first unit (3) being adapted to supply to the M outputs each time M samples that occur in consecutive blocks of M samples of the digitized input signal, such that the m-th sample of each block is supplied to the m-th output, each of the M outputs being coupled to an input of a corresponding one of M analysis filters (6.1 to 6.M), the synthesis filter means (16,19) further comprising a second unit (19) having M inputs (18.1 to 18.M) coupled to the M outputs of the synthesis filters (16.1 to 16.M) and an output (20) coupled to the output (21) of the synthesis filter means, the second unit (19) being adapted to arrange M samples, each time when they are present at the M inputs, one after the other in one block of consecutive blocks of M samples, such that the samples received at the m-th input are positioned in the m-th position in the consecutive blocks, the blocks being supplied to the output (20).

3. A system as claimed in Claim 1 or 2, characterized in that each analysis filter (6.m) comprises a series

arrangement (31) of delay sections having equal delay (T), the input of the filter being coupled to the input of the first delay section (32.1), outputs of at least a number of odd numbered delay sections (32.1, 32.3, ...) in the series arrangement being coupled to corresponding inputs of a first signal combination unit (33), outputs of least a number of even numbered delay sections (32.2,32.4,...) in the series arrangement being coupled to corresponding inputs of a second signal combination unit (34), outputs of the first and second signal combination unit being coupled to the first and second output (35.1,35.2) respectively of the filter.

4. A system as claimed in Claim 1 or 2, characterized in that each analysis filter comprises two series arrangements (40,41) of delay sections having equal delay (2T), the input (30) of the filter being coupled to the inputs (44.1,45.1) of the first and at least a number of other delay sections (44.2,45.2) in each series arrangement, the outputs of the two series arrangements being coupled to the first and second output (35.1,35.2) of the filter respectively, a further delay section (48) having a delay (T) that equals half the delay of the delay sections in the series arrangements, being coupled in the signal path from the input (30) to the second output (35.1) of the filter, the said further delay section not being included in the signal path from the input (30) to the first output (35.2) of the filter.

5. A system as claimed in Claim 3, characterized in that outputs of odd numbered delay sections being coupled to inputs of the first signal combination unit (33) only, and outputs of even numbered delay sections being coupled to inputs of the second signal combination unit only.

6. A system as claimed in Claim 3 or 5, characterized in that the outputs of the delay sections are coupled to the corresponding inputs of the first or second signal combination unit via multiplication units (a_{1m}, a_{2m},...).

7. A system as claimed in Claim 3, 5 or 6, characterized in that the filter input (30) is coupled to an input of the second signal combination unit (34) via a multiplication unit (a_{0m}).

8. A system as claimed in Claim 4, characterized in that the filter input (30) is coupled to the inputs of the delay sections (40,41) via multiplication units (b_{1m},c_{1m}).

9. A system as claimed in Claim 8, characterized in that an output of a multiplication unit (b_{2m}) is coupled to a first input a signal combination unit (46.1), a second input of the signal combination unit being coupled to an output of a delay section (44.1) in one of the two series arrangements, an output of the signal combination unit being coupled to an input of the next delay section (44.2) in the said series arrangement (40).

10. A system as claimed in Claim 4, 8 or 9, characterized in that the filter input (30) is coupled to the first and second output via a first and second signal path respectively, the said first and second signals paths each including a multiplication unit (b_{pm},c_{qm}) and being connected in parallel to the first and second series arrangement respectively.

11. A system as claimed in Claim 1 or 2, characterized in that each synthesis filter comprises tow series arrangements (52,53) of delay sections, having equal delay (2T), the first and second inputs (50.1,50.2) of the filter being coupled to an input of the first delay section of the first and second series arrangement respectively, outputs of at least a number of delay sections in the first series arrangement being coupled to corresponding inputs of a signal combination unit (54), outputs of at least a number of delay sections in the second series arrangement also being coupled to corresponding inputs of the signal combination unit, an output (60) of the signal combination unit being coupled to the filter output (51), a further delay section (55) having a delay (T) that equal half the delay of the delay sections in the series arrangements, being coupled in the signal path from the second input (50.2) to the ouptut (51) of the filter, the said further delay section not being included in the signal path from the first input (50.1) to the ouput (51) of the filter.

12. A system as claimed in Claim 1 or 2, characterized in that each synthesis filter comprises a series arrangement (65) of delay sections having equal delay (T), the first input (50.2) of the filter being coupled to inputs of at least a number of odd numbered delay sections (66.1,66.3,...) in the series arrangement, the second input (50.1) of the filter being coupled to inputs of at least a number of even numbered delay sections (66.2,66.4,...) in the series arrangement, the ouptut of the last delay section (66.n) being coupled to the output (15) of the filter.

13. A system as claimed in Claim 12, characterized in that the first filter input being coupled to inputs of odd numbered delay sections only, and the second filter input is coupled to inputs of even numbered delay sections only.

14. A system as claimed in Claim 11, characterized in that the outputs of the delay sections of the first and second series arrangements are coupled to corresponding inputs of the signal combination unit via multiplication units (d_{2m},d_{3m},e_{2m},e_{3m}).

15. A system as claimed in Claim 11 or 14, characterized in that the first and second filter input (50.2,50.1) are also coupled to corresponding inputs, of the signal combination unit via multiplication units (d_{1m},e_{1m}).

16. A system as claimed in Claim 12 or 13, characterized in that the filter inputs are coupled to the inputs of the delay sections via multiplication units (a_{1m},a_{2m},...).

17. A system as claimed in Claim 16, characterized in that an output of a signal multiplication unit (67.3) is coupled to a first input of a signal combination unit, a second input of the signal combination unit being coupled to an output of a delay section (66.2) in the series arrangement, an output of the signal combination unit being coupled to an input of the next delay section (66.3) in the series arrangement.

18. A system as claimed in Claim 12, 13, 16 or 17, characterized in that the second filter input (50.2) is coupled to the filter output (51) via signal path, the said signal path including a multiplication unit (a_{0m}) and being connected in parallel to the series arrangement.

19. A system as claimed in Claim 1 or 2, characterized in that the signal processing unit comprises M signal combination units (70.1,70.2,...) each having an output coupled to a corresponding one (74.i) of the M outputs of the signal processing unit, in that for each signal combination unit, at least a number of inputs (71.1,71.2,...) of the 2M inputs of the processing unit are coupled to corresponding inputs of the said signal combination unit (70.1), via corresponding multiplication units (72.11,72.12).

20. A system as claimed in Claim 1 or 2, characterized in that the other signal processing unit comprises 2M signal combination units (70.1,70.2,...), each having coupled to a corresponding one of the 2M outputs of the processing unit, in that, for each signal combination unit (74.i), at least a number of inputs (71.1,71.2,...) of the M inputs of the processing units are coupled to corresponding inputs of the said signal combination unit (70.1), via corresponding multiplication units (72.11,72.12).

21. A system as claimed in Claim 1 or 2, characterized in that the two outputs of each filter are each coupled to their corresponding inputs of the signal processing unit via a corresponding signal amplification unit (80.1,81.1), both amplification units being adapted to amplify the signals applied to their inputs by the same complex value (k_1).

22. A system as claimed in Claim 21, characterized in that the complex values (k_1,k_2,...) are different for amplification units coupled to different analysis filters.

23. A system as claimed in Claim 21 or 22, characterized in that each output (86.1) of the processing unit is coupled to its corresponding output (10.1) of the coder via a series arrangement of a signal amplification unit and real value determinator, the signal amplification unit being adapted to amplify the signal applied to its input by a complex value.

24. A system as claimed in Claim 1 or 2, characterized in that the two outputs (93.1,93.9) of each pair of outputs of the other signal processing unit (13′) are each coupled to their corresponding input of a synthesis filter (16.1) via a corresponding signal amplification unit (94.1,95.1), both amplification units being adapted to amplify the signals applied to their inputs the same complex value (k_1').

25. A system as claimed in Claim 24, characterized in that the complex values (k_1',k_2') are different for amplification units coupled to different synthesis filters (16.1,16.2).

26. A system as claimed in Claim 1 or 2, characterized in that the M inputs of the decoder are each coupled to their corresponding one of the M inputs of the other processing unit via a signal amplification unit

(90.1,90.2,...), the signal amplification unit being adapted to amplify the signal applied to its input by another complex value (v_1',v_2',...).

27. A system as claimed in Claim 23 or 26, characterized in that the other complex values are different from each other.

28. A system as claimed in any one of the Claims 6 to 10 and 14 to 20, characterized in that those multiplication units for which the multiplication factors with which they multiply their input signals, equal one, are dispensed with.

29. A system as claimed in any one of the Claims 6 to 10 and 14 to 20, characterized in that those couplings that include a multiplication unit for which the multiplication factor with which it multiplies its input signal, equals zero, are dispensed with.

30. A system as claimed in Claim 1 or 2, characterized in that signal processing unit (9″) comprises a switching means (100) and M signal combination units (102), each of the 2 M inputs (8.1 to 8.2M) of the signal processing unit being coupled to a corresponding one of 2 M inputs of the switching means, the switching means having one output (101) coupled to an input of each of the M signal combination units (102), each signal combination unit comprising a multiplication unit (106), a memory (107) having 2 M storage locations, an adder (108) and an accumulating register (109), the input of the signal combination unit and an output of the memory being coupled to a first and second input (112,111) respectively of the multiplication unit (106), an output of the multiplication unit and the accumulating register (109) being coupled to a first and second input (113,114) respectively of the adder (108), the adder having an output coupled to an input of the register, the ouput of the register (109) of the m-th signal combination unit being coupled to the m-th output (10.m) of the signal processing unit (9″), the switching means (100) being adapted to a cyclically couple each of its 2 M inputs (8.1 to 8.2M) with its output (10i), so as to apply each time the samples in blocks of 2 M samples that occur at its 2 M inputs, one sample at each input, serially to its output, the memory (107) comprising 2 M multiplication factors (α), the memory being adapted to supply in a circular fashion the 2 M multiplication factors to its output, in such a way that the i-th multiplication factor is supplied to its output, when the switching means (100) supplies the i-th sample of the 2 M samples in a block to its output, where i runs form 1 to 2 M, the adder (108) and accumulating register (109) being adapted to add the result ot the i-th multiplication to the contents contained in the accumulating register, the accumulating register further being adpated to supply its contents obtained after the 2 M-th multiplication step to the output (10.m) of the signal combination unit and to set its contents to zero thereafter.

31. A system as claimed in Claim 1 or 2, characterized in that the other signal processing unit comprises a switching means (100) and 2M signal combination units (102), each of the M inputs of the other signal processing unit being coupled to a corresponding one of M inputs of the switching means, the switching means having one output coupled to an input of each of the 2M signal combination units, each signal combination unit comprising a multiplication unit (106), a memory having M storage locations, an adder (108) and an accumulating register (109), the input of the signal combination unit and an output of the memory being coupled to a first and second input respectively of the multiplication unit (106), an output of the multiplication unit and the accumulating register being coupled to a first and second input respectively of the adder, the adder having an output coupled to an input of the register, the output of the register of the i-th signal combination unit being coupled to the i-th output of the other signal processing unit, where i runs from 1 to 2 M, the switching means being adapted to cyclically couple each of its M inputs with its output, so as to apply each time the samples in blocks of M samples that occur at its M inputs, one sample at each input, serially to its output, the memory comprising M multiplication factors, the memory being adapted to supply in a circular fashion the M multiplication factors to its output, in such a way that the m-th multiplication factor is supplied to its output, when the switching means applies the m-th sample of the M samples in a block to its output, the adder and accumulating register being adapted to add the result of the m-th multiplication to the contents contained in the accumulating register, the accumulating register further being adapted to supply its contents obtained after the M-th multiplicator step to the output (101) of the signal combination unit and to set its contents to zero thereafter.

32. A coder for subband coding of a digital signal, such as a digital audio signal, having a given sampling rate F_S, the coder being responsive to the digital signal, for generating a number of M subband signals with sampling rate reduction, the coder dividing the digital signal band into successive subbands of band num-

bers m($1 \leqq m \leqq M$) increasing with frequency, the coder (3,6,9) comprising analysis filter means (3,6) and a signal processing unit (9), the analysis filter means comprises M analysis filters (6.1 to 6.M) each having one input and two outputs, the 2M outputs on the filters being coupled to 2M outputs of the analysis filter means for supplying 2M output signals with a sampling rate F_S/M, each analysis filter (6.1) being adapted to apply two different filterings on the signal applied to its input (5.1) and to supply each of the two different filtered versions of that input signal to a corresponding one of the two outputs (7.1a, 7.2b), each one of the 2M filter outputs being coupled to a corresponding one of 2M inputs (8.1 to 8.2M) of a signal processing unit (9), the processing unit having M outputs (10.1 to 10.M) coupled to M outputs of the coder for supplying the M subband signals, the signal processing unit being adapted to supply output signals on each of M outputs, an output signal being a combination of at least a number of input signals applied to its 2M inputs, wherein the coder is adapted to divide the digital signal band into successive subbands (B_1, B_2, ...) having approximately equal bandwidths, characterized in that the coefficients of each of the analysis filters are derived from the coefficients of a standard filter (H(f)) having a low pass filter characteristic with a bandwidth approximately equal to half the bandwidth of the subbands, that the coefficients for the analysis filters are derived from a standard filter having an odd number of coefficients and that the coefficients for the analysis filters are derived from a standard filter having an odd number of coefficients, that M is an even number and that for making the number of coefficients of the standard filter equal to the number of multiplication factors of each of the analysis and synthesis filters, zeroes are added to the array of coefficients of the standard filter.

33. A decoder for decoding M subband signals that have been obtained by subband encoding a digital signal by dividing the digital signal band in approximately equal bandwidths, the decoder being responsive to the M subband signals for constructing a replica of the digital signal, this decoder merging the subbands to the digital signal band, with sampling rate increase, the decoder (13,16,19) comprising a signal processing unit (13) and synthesis filter means (16,19) the signal processing unit having M inputs (12.1 to 12.M) for receiving the M subband signals and having 2M outputs (14.1 to 14.2M), the synthesis filter means comprising M synthesis filters (16.1 to 16.M) each having 2 inputs, and one output (20) coupled to the decoder output, the other signal processing unit (13) being adapted to generate an output signal on each of its 2M outputs, an output signal being a combination of at least a number of input signals applied to its M inputs, each pair of outputs (14.1 to 14.2) of signal processing unit being coupled to a pair of two inputs (15.1a, 15.1b) of a corresponding one of the M synthesis filters (16.1 to 16.M), each synthesis filter (16.1) having one output (17.1), each synthesis filter being adapted to apply different filterings on the two signals applied to the two inputs and to supply a combination of the two filtered signals to its output, each output can be coupled to the output of the synthesis filter means for supplying the replica of the digital signal having a sampling rate F_S, characterized in that the coefficients of each of the synthesis filters are derived from the coefficients of a standard filter (H(f)) having alow pass filter characteristic with a bandwidth approximately equal to half the bandwidth of the subbands and that the coefficients for the synthesis filters are derived from a standard filter having an odd number of coefficients and that the coefficients for the synthesis filters are derived from a standard filter having an odd number of coefficients, that M is an even number and that for making the number of coefficients of the standard filter equal to the number of multiplication factors of each of the analysis and synthesis filters, zeroes are added to the array of coefficients of the standard filter.

34. A transmitter for transmitting a digital signal, including a coder (3,6,9) for subband coding of the digital signal according to claim 32.

35. A receiver for receiving a digital signal that have been encoded upon transmission into a number of M subband signals by dividing the digital signal band in subbands of approximately equal bandwidths with sampling rate reduction including a decoder according to claim 33.

36. A digital audio signal recording apparatus for recording a digital audio signal on a record carrier, comprising the transmitter as claimed in Claim 34, characterized in that it further comprises recording means (120) having M inputs (121.1 to 121.M), each one of the M inputs being coupled to a corresponding one of the M outputs (10.1 to 10.M) of the processing unit (9), the recording means being adapted to write the M subband signals applied to its M inputs in a track on the record carrier (122).

37. A digital audio signal reproduction apparatus for reproducing a digital audio signal from a record carrier, comprising the receiver as claimed in Claim 35, characterized in that it further comprises reproducing

means (124) having M outputs (125.1 to 125.M), each one of the M outputs being coupled to a corresponding one of the M inputs (12.1 to 12.M) of the processing unit (13), the reproducing means being adpated to read the M subband signals from a track on the record carrier (122).

Patentansprüche

1. Digitales Übertragungssystem mit einem Sender und einem Empfänger, wobei der Sender einen Coder (3,6,9) und der Empfänger einen Decoder (13,16,19) enthält, um ein digitales Signal im Teilband zu codieren, wie z.B. ein digitales Audiosignal mit einer gegebenen Abtastfrequenz F_S, wobei der Coder zum Erzeugen einer Anzahl von M Teilbandsignalen mit Abtastfrequenzverringerung auf das digitale Signal anspricht, und das Digitalsignalband in aufeinanderfolgende Teilbänder mit Bandnummern m($1 \leqq m \leqq M$) unterteilt, die mit der Frequenz ansteigen, wobei der Decoder auf die M Teilbandsignale zum Aufbauen einer Replik des digitalen Signals anspricht, und die Teilbänder zum Digitalsignalband mit Abtastfrequenzanstieg kombiniert, wobei der Coder (3,6,9) Analysefiltermittel (3,6) und eine Signalverarbeitungseinheit (9) enthält, wobei das Analysefiltermittel M Analysefilter (6.1 bis 6.M) enthält, die je einen Eingang und zwei Ausgänge besitzen, wobei die 2M Ausgänge der Filter mit 2M Ausgängen des Analysefiltermittels zur Auslieferung von 2M Ausgangssignalen mit einer Abtastfrequenz von F_S/M verbunden sind, wobei jedes Analysefilter (6.1) zum Durchführen von zwei verschiedenen Filterungen an dem an seinen Eingang (5.1) gelegten Signal und zum Ausliefern jedes der zwei verschiedenen filtrierten Ausführungen dieses Ausgangssignals an einen entsprechenden Ausgang der beiden Ausgänge (7.1a, 7.1b) ausgelegt ist, wobei jeder der 2M Filterausgänge an einen entsprechenden Eingang der 2M Eingänge (8.1 bis 8.2M) der Signalverarbeitungseinheit (9) angeschlossen ist, wobei die Verarbeitungseinheit mit M Ausgängen (10.1 bis 10.M) an M Ausgänge des Coders zum Ausliefern der M Teilbandsignale angeschlossen ist, wobei die Signalverarbeitungseinheit zur Lieferung von Ausgangssignalen an jeden der M Ausgänge ausgelegt ist, wobei ein Ausgangssignal eine Kombination wenigstens einer Anzahl von Eingangssignalen an seine 2M Eingänge ist, wobei der Decoder (13,16,19) eine andere Signalverarbeitungseinheit (13) und ein Synthesefiltermittel (16, 19) besitzt, wobei die andere Signalverarbeitungseinheit mit M Eingängen (12.1 bis 12.M) zum Empfangen der M Teilbandsignale und mit 2M Ausgängen (14.1 bis 14.2M) versehen ist, wobei das Synthesefiltermittel M Synthesefilter (16.1 bis 16.M) besitzt, die je 2 Eingänge enthalten, und mit einem Ausgang (20) an den Decoderausgang angeschlossen ist, wobei die andere Signalverarbeitungseinheit (13) zum Erzeugen eines Ausgangssignals an jedem seiner 2M Ausgänge ausgelegt ist, wobei ein Ausgangssignal eine Kombination wenigstens einer Anzahl von Eingangssignalen zu seinen M Eingängen ist, wobei jedes Ausgängepaar (14.1, 14.2) der anderen Signalverarbeitungseinheit an ein Paar von zwei Eingängen (15.1a, 15.1b) eines entsprechenden Filters der M Synthesefilters (16.1 bis 16.M) angeschlossen ist, wobei jedes Synthesefilter (16.1) einen Ausgang (17.1) besitzt, wobei jedes Synthesefilter zur Durchführung verschiedener Filterungen an den an die beiden Eingängen angelegten zwei Signalen und zur Lieferung einer Kombination der zwei gefiltereten Signale an seinem Ausgang ausgelegt ist, wobei jeder Ausgang an den Ausgang des Synthesefiltermittels zur Lieferung der Replik des digitalen Signals mit einer Abtastfrequenz von F_S verbindbar ist, daß der Coder zum Verteilen des Digitalsignalbandes in aufeinanderfolgende Teilbänder B_1, B_2, ...) mit etwa gleichen Bandbtreiten ausgelegt ist, dadurch gekennzeichnet, daß die Koeffizienten jedes der Analyse- und Synthesefilter aus den Koeffizienten eines Standardfilters (H(f)) mit einer Tiefpaßfilterkennlinie mit einer Bandbreite von etwa gleich der Hälfte der Bandbreite der Teilbänder abgeleitet sind, und daß die Koeffizienten jedes der Analyse- und Synthesefilter aus den Koeffizienten eines Standardfilters mit einer Tiefpaßfilterkennlinie mit einer Bandbreite etwa gleich der Hälfte der Bandbreite der Teilbänder abgeleitet sind, und daß die Koeffizienten für die Analysefilter und die Synthesefilter von einem Standardfilter mit einer ungeraden Anzahl Koeffizienten abgeleitet sind, daß M eine gerade Anzahl ist und daß zum Gleichmachen der Anzahl Koeffizienten des Standardfilters zu der Anzahl Multiplikationsfaktoren jedes der Analysefilter und Synthesefilter, zu der Reihe von Koeffizienten des Standardfilters Nullen hinzugefügt werden.

2. Digitales Übertragungssystem nach Anspruch 1, dadurch gekennzeichnet, daß das Analysefiltermittel (3,6) eine erste Einheit (3) mit einem an den Codereingang (1) angeschlossenen Eingang (2) zum Empfangen der Abtastungen des digitalen Signals und mit M Ausgängen (4.1 bis 4.M) zum Ausgeben von M Ausgangssignalen mit einer Abtastfrequenz von F_S/M enthält, wobei die erste Einheit (3) zum jeweiligen Ausgeben von M Abtastungen ausgelegt ist, die in aufeinanderfolgenden Blöcken von M Abtastungen des digitalisierten Eingangssignals derart erscheinen, daß die m. Abtastung jedes Blocks an den m. Ausgang gelangt, wobei jeder der M Ausgänge mit einem Eingang eines entsprechenden Filters von M Analysefil-

tern (6.1 bis 6.M) gekoppelt ist, wobei das Synthesefiltermittel (16, 19) außerdem eine zweite Einheit (19) mit M Eingängen (18.1 bis 18.M) enthält, die mit den M Ausgängen der Synthesefilter (16.1 bis 16.M) und ein Ausgang (20) mit dem Ausgang (21) des Synthesefiltermittels gekoppelt sind, die zweite Einheit (19) jedesmal beim Vorliegen der Abtastungen an den M Eingängen zum Ordnen von M Abtastungen eine nach der anderen in einem Block aufeinanderfolgender Blöcke von M Abtastungen derart ausgelegt ist, daß die am m. Eingang empfangenen Abtastungen sich an der m. Stelle in den aufeinanderfolgenden Blöcken befinden, wonach die Blöcke an den Ausgang (20) gelangen.

3. Digitales Übertragungssustem nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß jedes Analysefilter (6.M) eine Reihenschaltung (31) von Verzögerungsabschnitten mit gleicher Verzögerung (T) enthält, wobei der Filtereingang an den Eingang des ersten Verzögerungsabschnitts (32.1) angeschlossen ist, Ausgänge wenigstens einer Anzahl ungeradzahliger Verzögerungsabschnitte (32.1, 32.3, ...) in der Reihenschaltung an entsprechende Eingänge einer ersten Signalverknüpfungseinheit (33) angeschlossen sind, Ausgänge wenigstens einer Anzahl geradzahliger Verzögerungsabschnitte (32.2, 32.4, ...) in der Reihenschaltung an entsprechende Eingänge einer zweiten Signalverknüpfungseinheit (34) angeschlossen sind, Ausgänge der ersten und der zweiten Signalverknüpfungseinheit an den ersten bzw. den zweiten Ausgang (35.1, 35.2) des Filters angeschlossen sind.

4. System nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß jedes Analysefilter zwei Reihenschaltungen (40, 41) von Verzögerungsabschnitten mit gleichem Verzögerungsbetrag (2T) enthält, wobei der Eingang (30) des Filters an die Eingänge (44.1, 45.1) der ersten und wenigstens eine Anzahl anderer Verzögerungsabschnitte (44.2, 45.2) in jeder Reihenschaltung und die Ausgänge der beiden Reihenschaltungen an den ersten bzw. zweiten Filterausgang (35.1, 35.2) angeschlossen sind, wobei ein weiterer Verzögerungsabschnitt (48) mit einer Verzögerung (T) gleich der Hälfte der Verzögerung der Verzögerungsabschnitte in den Reihenschaltungen in dem Signalweg vom Eingang (30) zum zweiten Filterausgang (35.1) verbunden ist, wobei der weitere Verzögerungsabschnitt nicht in den Signalweg vom Eingang (30) zum ersten Filterausgang (35.2) aufgenommen ist.

5. System nach Anspruch 3, dadurch gekennzeichnet, daß Ausgänge ungeradzahliger Verzögerungsabschnitte mit Eingängen der ersten Signalverknüpfungseinheit (33) allein gekoppelt ist, und daß Ausgänge geradzahliger Verzögerungsabschnitte mit Eingängen der zweiten Signalverknüpfungseinheit allein gekoppelt sind.

6. System nach Anspruch 3 oder 5, dadurch gekennzeichnet, daß die Ausgänge der Verzögerungsabschnitte mit den entsprechenden Eingängen der ersten oder zweiten Signalverknüpfungseinheit über Vervielfachungseinheiten (a_{1m}, a_{2m}, ...) gekoppelt sind.

7. System nach Anspruch 3, 5 oder 6, dadurch gekennzeichnet, daß der Filtereingang (30) mit einem Eingang der zweiten Signalverknüpfungseinheit (34) über eine Vervielfachungseinheit (a_{0m}) gekoppelt ist.

8. System nach Anspruch 4, dadurch gekennzeichnet, daß der Filtereingang (30) mit den Eingängen der Verzögerungsabschnitte (40, 41) über Vervielfachungseinheiten (b_{1m}, c_{1m}) gekoppelt sind.

9. System nach Anspruch 8, dadurch gekennzeichnet, daß ein Ausgang einer Vervielfachungseinheit (b_{2m}) mit einem ersten Eingang einer Signalverknüpfungseinheit (46.1) gekoppelt, ein zweiter Eingang der Signalverknüpfungseinheit mit einem Ausgang eines Verzögerungsabschnitts (44.1) in einer der zwei Reihenschaltungen und ein Ausgang der Signalverknüpfungseinheit mit einem Eingang des folgenden Verzögerungsabschnitts (44.2) in der betreffenden Reihenschaltung (40) gekoppelt sind.

10. System nach Anspruch 4, 8 oder 9, dadurch gekennzeichnet, daß der Filtereingang (30) mit dem ersten und dem zweiten Ausgang über einen ersten bzw. einen zweiten Signalweg gekoppelt ist, wobei diese ersten und zweiten Signalwege je eine Vervielfachungseinheit (b_{Am}, c_{qm}) enthalten und zur ersten bzw. zweiten Reihenschaltung parallelgeschaltet sind.

11. System nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß jedes Synthesefilter zwei Reihenschaltungen (52, 53) von Verzögerungsabschnitten mit gleichem Verzögerungsbetrag (2T) enthält, wobei die ersten und zweiten Filtereingänge (50.1, 50.2) mit einem Eingang des ersten Verzögerungsabschnitts der ersten bzw. der zweiten Reihenschaltung verbunden sind, Ausgänge wenigstens einer Anzahl von Ver-

zögerungsabschnitten in der ersten Reihenschaltung mit entsprechenden Eingängen einer Signalverknüpfungseinheit (54) verbunden sind, Ausgänge wenigstens einer Anzahl von Verzögerungsabschnitten in der zweiten Reihenschaltung ebenfalls mit entsprechenden Eingängen der Signalverknüpfungseinheit gekoppelt sind, ein Ausgang (60) der Signalverknüpfungseinheit an den Filterausgang (51) angeschlossen ist, ein weiterer Verzögerungsabschnitt (55) mit einer Verzögerung (T) gleich der Hälfte der Verzögerung der Verzögerungsabschnitte in den Reihenschaltungen in den Signalweg vom zweiten Eingang (50.2) zum Filterausgang (51) aufgenommen ist, und der weitere Verzögerungsabschnitt nicht in den Signalweg vom ersten Eingang (50.1) zum Filterausgang (51) aufgenommen ist.

12. System nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß jedes Synthesefilter eine Reihenschaltung (65) von Verzögerungsabschnitten mit gleicher Verzögerung (T) enthält, der erste Filtereingang (50.2) an Eingänge wenigstens einer Anzahl ungeradzahliger Verzögerungsabschnitte (66.1, 66.3,...) in der Reihenschaltung gekoppelt sind, der zweite Filtereingang (50.1) mit Eingängen wenigstens einer Anzahl geradzahliger Verzögerungsabschnitte (66.2, 66.4, ...) in der Reihenschaltung gekoppelt sind und der Ausgang des letzten Verzögerungsabschnitts (66.n) an den Filterausgang (15) angeschlossen ist.

13. System nach Anspruch 12, dadurch gekennzeichnet, daß der erste Filtereingang an Eingänge nur ungeradzahliger Verzögerungsabschnitte angeschlossen und der zweite Filtereingang mit Eingängen nur geradzahliger Verzögerungsabschnitte gekoppelt ist.

14. System nach Anspruch 11, dadurch gekennzeichnet, daß die Ausgänge der Verzögerungsabschnitte der ersten und zweiten Reihenschaltungen mit entsprechenden Eingängen der Signalverknüpfungseinheit über Vervielfachungseinheiten (2_{2m}, d_{3m}, e_{2m}, e_{3m}) gekoppelt sind.

15. System nach Anspruch 11 oder 14, dadurch gekennzeichnet, daß der erste und der zweite Filtereingang (50.2, 50.1) ebenfalls mit entsprechenden Eingängen der Signalverknüpfungseinheit über Vervielfachungseinheiten (d_{1m}, e_{1m}) gekoppelt sind.

16. System nach Anspruch 12 oder 13, dadurch gekennzeichnet, daß die Filtereingange über Vervielfachungseinheiten (a_{1m}, a_{2m}, ...) mit den Eingängen der Verzögerungsabschnitte gekoppelt sind.

17. System nach Anspruch 16, dadurch gekennzeichnet, daß ein Ausgang einer Vervielfachungseinheit (67.3) mit einem ersten Eingang einer Signalverknüpfungseinheit gekoppelt, ein zweiter Eingang der Signalverknüpfungseinheit mit einem Ausgang eines Verzögerungsabschnitts (66.2) in der Reihenschaltung und ein Ausgang der Signalverknüpfungseinheit mit einem Eingang des folgenden Verzögerungsabschnitts (66.3) in der betreffenden Reihenschaltung gekoppelt sind.

18. System nach Anspruch 12, 13, 16 oder 17, dadurch gekennzeichnet, daß der zweite Filtereingang (50.2) über einen Signalweg mit dem Filterausgang (51) gekoppelt ist, dieser Signalweg eine Vervielfachungseinheit (a_{0m}) enthält und zur Reihenschaltung parallelgeschaltet ist.

19. System nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Signalverarbeitungseinheit M Signalverknüpfungseinheiten (70.1, 70.2, ...) enthält, die mit je einem Ausgang an einen entsprechenden Ausgang (74.1) der M Ausgänge der Signalverarbeitungseinheit angeschlossen sind, daß für jede Signalverknüpfungseinheit wenigstens eine Anzahl von Eingängen (71.1, 71.2, ...) von den 2M Eingängen der Verarbeitungseinheit mit entsprechenden Eingängen dieser Signalverknüpfungseinheit (70.1) über entsprechende Vervielfachungseinheiten (72.11, 72.12) gekoppelt sind.

20. System nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die andere Signalverarbeitungseinheit 2M Signalverknüpfungseinheiten (70.1, 70.2, ...) enthält, die mit je einem Ausgang an einen entsprechenden Ausgang der 2M Ausgänge der Verarbeitungseinheit gekoppelt sind, daß für jede Signalverknüpfungseinheit (74.i) wenigstens eine Anzahl von Eingängen (71.1, 71.2, ...) der M Eingänge der Verarbeitungseinheiten an entsprechende Eingänge dieser Signalverknüpfungseinheit (70.1) über entsprechende Vervielfachungseinheiten (72.11, 72.12) angeschlossen sind.

21. System nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die zwei Ausgänge jedes Analysefilters mit ihren entsprechenden Eingängen der Signalverarbeitungseinheit über eine entsprechende Signalverstärkungseinheit (80.1, 81.1) gekoppelt sind, wobei beide Verstärkungseinheiten zum Verstärken der an

ihre Eingänge angelegten Signale um denselben komplexen Wert (K_1) ausgelegt sind.

22. System nach Anspruch 21, dadurch gekennzeichnet, daß die komplexen Werte (K_1, K_2, ...) für an verschiedene Analysefilter angeschlossene Verstärkungseinheiten abweichen.

23. System nach Anspruch 21 oder 22, dadurch gekennzeichnet, daß jeder Ausgang (86.1) der Verarbeitungseinheit an seinen entsprechenden Coderausgang (10.1) über eine Reihenschaltung einer Signalverstärkungseinheit und einen Realwertbestimmer gekoppelt ist, wobei die Signalverstärkungseinheit zum Verstärken des an seinen Eingang gelegten Signals um einen komplexen Wert ausgelegt ist.

24. System nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die zwei Ausgänge (93.1, 93.2) jedes Ausgängepaars der anderen Signalverarbeitungseinheit (13′) mit ihrem entsprechenden Eingang eines Synthesefilters (16.1) über eine entsprechende Signalverstärkungseinheit (94.1, 95.1) gekoppelt sind, wobei beide Verstärkungseinheiten zum Verstärken der an ihre Eingänge gelegten Signale um denselben komplexen Wert (K_1')ausgelegt sind.

25. System nach Anspruch 24, dadurch gekennzeichnet, daß die komplexen Werte (K_1', K_2') für Verstärkungseinheiten, die mit verschiedenen Synthesefiltern (16.1, 16.2) gekoppelt sind, abweichen.

26. System nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die M Eingänge des Decoders an ihren entsprechenden Eingang der M Eingänge der anderen Verarbeitungseinheit über eine Signalverstärkungseinheit angeschlossen sein, wobei die Signalverstärkungseinheit (90.1, 90.2, ...) zum Verstärken des an seinen Eingang gelegten Signals um einen weiteren komplexen Wert (V_1', V_2', ...) ausgelegt ist.

27. System nach Anspruch 23 oder 26, dadurch gekennzeichnet, daß die anderen komplexen Werte voneinander abweichen.

28. System nach einem oder mehreren der Ansprüche 6 bis 10 sowie 14 bis 20, dadurch gekennzeichnet, daß diejenigen Vervielfachungseinheiten, deren Vervielfachungsfaktoren zum Vervielfachen ihrer Eingangssignale gleich eins sind, abkömmlich sind.

29. System nach einem der Ansprüche 6 bis 10 und 14 bis 20, dadurch gekennzeichnet, daß diejenigen Kopplungen, die eine Vervielfachungseinheit enthalten, deren Vervielfachungsfaktor zum Vervielfachen ihres Eingangssignals gleich Null ist, abkömmlich sind.

30. System nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Signalverarbeitungseinheit (9″) ein Schaltmittel (100) und M Signalverknüpfungseinheiten (102) enthält, wobei jeder der 2M Eingänge (8.1 bis 8.2M) der Signalverarbeitungseinheit an einen entsprechenden Eingang von 2M Eingängen des Schaltmittels angeschlossen sind, wobei der eine Ausgang (101) des Schaltmittels mit einem Eingang jedes der M Signalverknüpfungseinheiten (102) gekoppelt ist, wobei jede Signalverknüpfungseinheit eine Vervielfachungseinheit (106) enthält, wobei ein Speicher (107) mit 2M Speicherstellen, einen Addierer (108) und ein Saldierregister (109) besitzt, wobei der Eingang der Signalverknüpfungseinheit und ein Speicherausgang an einen ersten bzw. einen zweiten Eingang (112 bzw. 111) der Vervielfachungseinheit angeschlossen sind, ein Ausgang der Vervielfachungseinheit (106) und das Saldierregister (109) an einen ersten bzw. einen zweiten Eingang (113, 114) des Addierers (108) angeschlossen sind, ein Ausgang des Addierers mit einem Eingang des Registers gekoppelt ist, der Ausgang des Registers (109) der m. Signalverknüpfungseinheit mit dem m. Ausgang (10.m) der Signalverarbeitungseinheit (9″) gekoppelt ist, das Schaltmittel (100) zum zyklischen Koppeln jedes seiner 2M Eingänge (8.1 bis 8.2M) mit seinem Ausgang (10_i) ausgelegt ist, um jeweils die Abtastungen in Blöcken von 2M Abtastungen, die an seinen 2M Eingängen erscheinen, je eine Abtastung an jeden Eingang, seriell seinem Ausgang zuzuführen, der Speicher (107) 2M Vervielfachungsfaktoren (α) enthält und zum Zuleiten der 2M Vervielfachungsfaktoren auf kreisförmige Weise zu seinem Ausgang derart ausgelegt ist, daß der i. Vervielfachungsfaktor seinem Ausgang zugeleitet wird, wenn das Schaltmittel (100) die i. Abtastung der 2M Abtastung in einem Block seinem Ausgang zuführt, worin i von 1 bis 2M lauft, der Addierer (108) und das Saldierregister (109) zum Addieren des Ergebnisses der i. Multiplikation beim Inhalt im Saldierregister aufzählt, und das Saldierregister außerdem zum Ausgeben seines Inhalts nach dem 2M. Vervielfachungsschritt an den Ausgang (10.m) der Signalverknüpfungseinheit und zum anschließenden Nullrückstellen seines Inhalts ausgelegt ist.

31. System nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die andere Signalverarbeitungseinheit ein Schaltmittel (100) und 2M Signalverknüpfungseinheiten (102) enthält, wobei jeder der M Eingänge der anderen Signalverarbeitungseinheit an einen entsprechenden Eingang von M Eingängen des Schaltmittels angeschlossen ist, der einen Ausgang des Schaltmittels mit einem Eingang jedes der 2M Signalverknüpfungseinheiten gekoppelt ist, jede Signalverknüpfungseinheit eine Vervielfachungseinheit (106) enthält, ein Speicher mit M Speicherstellen, einen Addierer (108) und ein Saldierregister (109) besitzt, wobei der Eingang der Signalverknüpfungseinheit und ein Speicherausgang an einen ersten bzw. einen zweiten Eingang der Vervielfachungseinheit (106) angeschlossen sind, ein Ausgang der Vervielfachungseinheit und das Saldierregister an einen ersten bzw. einen zweiten Eingang des Addierers angeschlossen sind, ein Ausgang des Addierers mit einem Eingang des Registers gekoppelt ist, der Ausgang des Registers der i. Signalverknüpfungseinheit mit dem i. Ausgang der anderen Signalverarbeitungseinheit qekoppelt ist, worin i von 1 bis 2M läuft, das Schaltmittel züm zyklischen Koppeln jedes seiner M Eingänge mit seinem Ausgang ausgelegt ist, um jeweils die Abtastungen in Blöcken von M Abtastungen, die an seinen M Eingängen erscheinen, je eine Abtastung an jeden Eingang, seriell seinem Ausgang zuzuführen, der Speicher M Vervielfachungsfaktoren enthält und zum Zuleiten der M Vervielfachungsfaktoren auf kreisförmige Weise zu seinem Ausgang derart ausgelegt ist, daß der m. Vervielfachungsfaktor seinem Ausgang zugeleitet wird, wenn das Schaltmittel die m. Abtastung der M Abtastungen in einem Block seinem Ausgang zuführt, der Addierer und das Saldierregister zum Addieren des Ergebnisses der m. Multiplikation beim Inhalt im Saldierregister aufzählt, und das Saldierregister außerdem zum Ausgeben seines Inhalts nach dem M. Vervielfachungsschritt an den Ausgang (101) der Signalverknüpfungseinheit und zum anschließenden Nullrückstellen seines Inhalts ausgelegt ist.

32. Coder zur Teilbandcodierung eines digitalen Signals, wi eines digitalen Audiosignals mit einer bestimmten Abtastrate F_S, wobei der Coder auf das Digitale Signal anspricht zum Erzeugen einer Anzahl M Teilbandsignale mit Abtastratenverringerung, wobei der Coder das digitale Signalband in aufeinanderfolgende Teilbänder mit Bandnummern m($1 \leqq m \leqq M$), die mit der Frequenz ansteigen, aufteilt, wobei der Coder (3,6,9) Analysefiltermittel (3,6) und eine Signalverarbeitungseinheit (9) enthält, das Analysefiltermittel M Analysefilter (6.1 bis 6.M) enthält, die je einen Eingang und zwei Ausgänge besitzen, wobei die 2M Ausgänge auf den Filtern mit 2M Ausgängen des Analysefiltermittels zur Auslieferung von 2M Ausgangssignalen mit einer Abtastrate von F_S/M verbunden sind, wobei jedes Analysefilter (6.1) zum Durchführen von zwei verschiedenen Filterungen an dem an seinen Eingang (5.1) gelegten Signal und zum Ausliefern jedes der zwei verschiedenen filtrierten Ausführungen dieses Ausgangssignals an einen entsprechenden Ausgang der beiden Ausgänge (7.1a, 7.2b) ausgelegt ist, wobei jeder der 2M Filterausgänge an einen entsprechenden Eingang der 2M Eingänge (8.1 bis 8.2M) einer Signalverarbeitungseinheit (9) angeschlossen ist, wobei die Verarbeitungseinheit mit M Ausgängen (10.1 bis 10.M) an M Ausgänge des Coders zum Ausliefern der M Teilbandsignale angeschlossen ist, wobei die Signalverarbeitungseinheit zur Lieferung von Ausgangssignalen an jeden der M Ausgänge ausgelegt ist, wobei ein Ausgangssignal eine Kombination wenigstens einer Anzahl von Eingangssignalen an seine 2M Eingänge ist, wobei der Coder dazu vorgesehen ist, das digitale Signalband in aufeinanderfolgende Teilbänder (B_1, B_2, ...) mit nahezu gleichen Bandbreiten aufzuteilen, dadurch gekennzeichnet, daß die Koeffizienten jedes der Analysefilter aus den Koeffizienten eines Standardfilters (H(f)) mit einer Tiefpaßfilterkennlinie mit einer Bandbreite etwa gleich der Hälfte der Bandbreite der Teilbänder abgeleitet sind, und daß die Koeffizienten für die Analysefilter von einem Standardfilter mit einer ungeraden Anzahl Koeffizienten abgeleitet sind, daß M eine gerade Anzahl ist und daß zum Gleichmachen der Anzahl Koeffizienten des Standardfilters zu der Anzahl Multiplikationsfaktoren jedes der Analysenfilter und Synthesefilter, zu der Reihe von Koeffizienten des Standardfilters Nullen hinzugefügt werden.

33. Decoder zum Decodieren von M Teilbandsignals, die durch Teilbandcodierung eines digitalen Signals erhalten worden sind durch Aufteilung des digitalen Signalbandes in etwa gleiche Bandbreiten, wobei der Decoder auf die M Teilbandsignale zum Aufbauen einer Replik des digitalen Signals anspricht und die Teilbänder zum Digitalsignalband mit Abtastgeschwindigkeitsanstieg kombiniert, wobei der Decoder (13,16,19) eine Signalverarbeitungseinheit (13) und ein Synthesefiltermittel (16,19) besitzt, wobei die Signalverarbeitungseinheit mit M Eingängen (12.1 bis 12.M) zum Empfangen der M Teilbandsignale und mit 2M Ausgängen (14.1 bis 14.M) versehen ist, wobei das Synthesefiltermittel M Synthesefilter (16.1 bis 16.M) besitzt, die je 2 Eingänge enthalten, und mit einem Ausgang (20) an den Decoderausgang angeschlossen ist, wobei die andere Signalverarbeitungseinheit (13) zum Erzeugen eines Ausgangssignals an jedem seiner 2M Ausgänge ausgelegt ist, wobei ein Ausgangssignal eine Kombination wenigstens einer Anzahl von Eingangssignalen zu seinen M Eingängen ist, wobei jedes Ausgängepaar (14.1 bis 14.2)

der Signalverarbeitungseinheit an ein Paar von zwei Eingängen (15.1a, 15.1b) eines entsprechenden Filters der M Synthesefilter (16.1 bis 16.M) angeschlossen ist, wobei jedes Synthesefilter (16.1) einen Ausgang (17.1) besitzt, wobei jedes Synthesefilter zur Durchführung verschiedener Filterungen an den den beiden Eingängen zugeführten zwei Signalen und zur Lieferung einer Kombination der zwei gefilterten Signalen an seinen Ausgang ausgelegt ist, wobei jeder Ausgang an den Ausgang des Synthesefiltermittels zur Lieferung der Replik des digitalen Signals mit einer Abtastrate von F_S verbindbar ist, dadurch gekennzeichnet, daß die Koeffizienten jedes der Synthesefilter aus den Koeffizienten eines Standardfilters mit einer Tiefpaßfilterkennlinie mit einer Bandbreite etwa gleich der Hälfte der Bandbreite der Teilbänder abgeleitet sind, und daß die Koeffizienten für die Synthesefilter von einem Standardfilter mit einer ungeraden Anzahl Koeffizienten abgeleitet sind, daß M eine gerade Anzahl ist und daß zum Gleichmachen der Anzahl Koeffizienten des Standardfilters zu der Anzahl Multiplikationsfaktoren jedes der Analyse- und Synthesefilter, zu der Reihe von Koeffizienten des Standardfilters Nullen hinzugefügt werden.

34. Sender zum Übertragen eines digitalen Signals mit einem Coder (3,6,9) zur Teilbandcodierung des digitalen Signals nach Anspruch 32.

35. Empfänger zum Empfangen eines digitalen Signals, das bei der Übertragung in eine Anzahl von M Teilbandsignale aufgeteilt worden ist durch Teilung des digitalen Signalbandes in Teilbänder etwa gleicher Bandbreite mit Abtastratenverringerung mit einem Decoder nach Anspruch 33.

36. Digitales Audiosignal-Aufzeichnungsgerät zum Aufzeichnen eines digitalen Audiosignals auf einem Aufzeichnungsträger, mit dem Sender nach Anspruch 34, dadurch gekennzeichnet, daß im Gerät außerdem Aufzeichnungsmittel (120) mit M Eingängen (121.1 bis 121.M) vorgesehen sind, wobei jeder der M Eingänge mit einem entsprechenden Ausgang der M Ausgänge (10.1 bis 10.M) der Signalverarbeitungseinheit (9) gekoppelt ist, wobei die Aufzeichnungsmittel zum Einschreiben der M Teilbandsignale zu seinen M Eingängen in eine Spur auf dem Aufzeichnungsträger (122) ausgelegt ist.

37. Digitales Audiosignal-Wiedergabegerät zum Auslesen eines digitalen Audiosignals aus einem Aufzeichnungsträger, mit dem Empfänger nach Anspruch 35, dadurch gekennzeichnet, daß im Gerät außerdem Wiedergabemittel (124) mit M Ausgängen (125.1 bis 125.M) vorgesehen sind, wobei jeder der M Ausgänge mit einem entsprechenden Eingang der M Eingänge (12.1 bis 12.M) der Signalverarbeitungseinheit (13) gekoppelt ist, wobei die Wiedergabemittel zum Auslesen der M Teilbandsignale aus einer Spur auf dem Aufzeichnungsträger (122) ausgelegt ist.

Revendications

1. Système de transmission numérique comportant un émetteur et un récepteur, l'émetteur comprenant un codeur (3, 6, 9) et le récepteur comprenant un décodeur (13, 16, 19), pour le codage en sous-bandes d'un signal numérique, tel qu'un signal audionumérique, ayant une cadence d'échantillonnage donnée Fs, le codeur étant sensible au signal numérique pour générer un nombre M de signaux de sous-bandes avec une réduction de la cadence d'échantillonnage, le codeur divisant la bande de signaux numériques en des sous-bandes successives de nombres de bandes m($1 \leqq m \leqq M$) augmentant avec la fréquence, le décodeur étant sensible aux M signaux de sous-bandes pour construire une réplique du signal numérique, ce décodeur fusionnant les sous-bandes dans la bande de signal numérique, avec une augmentation de la cadence d'échantillonnage, système dans lequel le codeur (3, 6, 9) comprend des moyens de filtrage par analyse (3, 6) et une unité de traitement de signaux (9), les moyens de filtrage par analyse comprennent M filtres d'analyse (6.1 à 6.M) ayant chacun une entrée et deux sorties, les 2M sorties des filtres étant couplées à 2M sorties des moyens de filtrage par analyse pour délivrer 2M signaux de sortie avec une cadence d'échantillonnage F_S/M, chaque filtre d'analyse (6.1) étant à même d'appliquer deux filtrages différents au signal appliqué à son entrée (5.1) et de délivrer chacune des deux versions filtrées différentes de ce signal d'entrée à une sortie correspondante des deux sorties (7.1a, 7.1b), chacune des 2M sorties des filtres étant couplée à une entrée correspondante des 2M entrées (8.1 à 8.2M) d'une unité de traitement de signaux (9), l'unité de traitement ayant M sorties (10.1 à 10.M) couplées à M sorties du codeur pour délivrer les M signaux de sous-bandes, l'unité de traitement de signaux étant à même de délivrer des signaux de sortie à chacune des M sorties, un signal de sortie étant une combinaison d'au moins un certain nombre de signaux d'entrée appliqués à ses 2M entrées, le décodeur (13, 16, 19) comprend une autre unité de traitement de signaux (13) et des moyens de filtrage par synthèse (16, 19),

l'autre unité de traitement de signaux comportant M entrées (12.1 à 12.M) pour recevoir les M signaux de sous-bandes et 2M sorties (14.1 à 14.2M), les moyens de filtrage par synthèse comprenant M filtres de synthèse (16.1 à 16.M) comportant chacun deux entrées, et une sortie (20) couplée à la sortie du décodeur, l'autre unité de traitement de signaux (13) étant à même de générer un signal de sortie à chacune de ses 2M sorties, un signal de sortie étant une combinaison d'au moins un certain nombre de signaux d'entrée appliqués à ses M entrées, chaque paire de sorties (14.1, 14.2) de l'autre unité de traitement de signaux étant couplée à une paire de deux entrées (15.1a, 15.1b) d'un filtre correspondant des M filtres de synthèse (16.1 à 16.M), chaque filtre de synthèse ayant une sortie (17.1), chaque filtre de synthèse étant à même d'appliquer différents filtrages sur les deux signaux appliqués aux deux entrées et de délivrer une combinaison des deux signaux filtrés à sa sortie, chaque sortie peut être couplée à la sortie des moyens de filtrage par synthèse pour délivrer la réplique du signal numérique ayant une cadence d'échantillonnage F_s, le codeur est à même de diviser la bande de signaux numériques en sous-bandes (B1, B2, ...) successives ayant des largeurs approximativement égales, caractérisé en ce que les coefficients de chacun des filtres d'analyse et de synthèse sont dérivés des coefficients d'un filtre standard (H(f)) ayant une caractéristique de filtrage passe-bas avec une largeur de bande approximativement égale à la moitié de la largeur des sous-bandes, et les coefficients pour les filtres d'analyse et les filtres de synthèse sont dérivés d'un filtre standard ayant un nombre impair de coefficients, M est un nombre pair et, pour faire en sorte que le nombre de coefficients du filtre standard soit égal au nombre de facteurs de multiplication de chacun des filtres d'analyse et de synthèse, des zéros sont ajoutés à l'ensemble de coefficients du filtre standard.

2. Système de transmission numérique selon la revendication 1, caractérisé en ce que les moyens de filtrage d'analyse (3, 6) comprennent une première unité (3) ayant une entrée (2) couplée à l'entrée (1) du codeur, pour recevoir les échantillons du signal numérique et M sorties (4.1 à 4.M) pour délivrer M signaux de sortie avec une cadence d'échantillonnage de F_s/M, la première unité (3) étant à même de délivrer aux M sorties chaque fois M échantillons qui se présentent dans des blocs consécutifs de M échantillons du signal d'entrée numérisé, de telle sorte que le $m^{ème}$ échantillon de chaque bloc soit délivré à la $m^{ème}$ sortie, chacune des M sorties étant couplée à une entrée d'un filtre correspondant de M filtres d'analyse (6.1 à 6.M), les moyens de filtrage par synthèse (16, 19) comprenant, en outre, une deuxième unité (19) ayant M entrées (18.1 à 18.M) couplées aux M sorties des filtres de synthèse (16.1 à 16.M) et une sortie (20) couplée à la sortie (21) des moyens de filtrage par synthèse, la deuxième unité (19) étant à même d'agencer M échantillons, chaque fois qu'ils sont présents aux M entrées, l'un après l'autre dans un bloc parmi des blocs consécutifs de M échantillons, de telle sorte que les échantillons reçus à la $m^{ème}$ entrée soient disposés dans la $m^{ème}$ position dans les blocs consécutifs, les blocs étant délivrés à la sortie (20).

3. Système selon la revendication 1 ou 2, caractérisé en ce que chaque filtre d'analyse (6.m) comprend un agencement en série (31) de sections à retard ayant un retard égal (T), l'entrée du filtre étant couplée à l'entrée de la première section à retard (32.1), des sorties d'au moins un certain nombre de sections à retard impaires (32.1, 32.3, ...) du montage en série étant couplées à des entrées correspondantes d'une première unité de combinaison de signaux (33), des sorties d'au moins un certain nombre de sections à retard paires (32.2, 32.4, ...) du montage en série étant couplées à des entrées correspondantes d'une deuxième unité de combinaison de signaux (34), des sorties de la première et de la deuxième unités de combinaison de signaux étant couplées à la première et la deuxième sorties (35.1, 35.2), respectivement, du filtre.

4. Système selon la revendication 1 ou 2, caractérisé en ce que chaque filtre d'analyse comprend deux montages en série (40, 41) de sections à retard ayant un retard égal (2T), l'entrée (30) du filtre étant couplée aux entrées (44.1, 45.1) de la première et d'au moins un certain nombre d'autres sections à retard (44.2, 45.2) de chaque montage en série, les sorties des deux montages en série étant couplées à la première et à la deuxième sorties (35.1, 35.2) du filtre, respectivement, une autre section à retard (48) ayant un retard (T), qui est égal à la moitié du retard des sections à retard des montages en série, étant couplée dans le trajet de signaux allant de l'entrée (30) à la deuxième sortie (35.1) du filtre, ladite autre section à retard n'étant pas incluse dans le chemin de signaux allant de l'entrée (30) à la première sortie (35.2) du filtre.

5. Système selon la revendication 3, caractérisé en ce que des sorties de sections à retard impaires sont couplées à des entrées de la première unité de combinaison de signaux (33) uniquement et des sorties de sections à retard paires sont couplées à des entrées de la deuxième unité de combinaison de signaux

uniquement.

6. Système selon la revendication 3 ou 5, caractérisé en ce que les sorties des sections à retard sont couplées aux entrées correspondantes de la première ou de la deuxième unité de combinaison de signaux via des unités de multiplication (a_{1m}, a_{2m},...).

7. Système selon la revendication 3, 5 ou 6 caractérisé en ce que l'entrée (30) du filtre est couplée à une entrée de la deuxième unité de combinaison de signaux (34) via une unité de multiplication (a_{0m}).

8. Système selon la revendication 4, caractérisé en ce que l'entrée (30) du filtre est couplée aux entrées des sections à retard (40, 41) via des unités de multiplication (b_{1m}, c_{1m}).

9. Système selon la revendication 8, caractérisé en ce qu'une sortie d'une unité de multiplication (b_{2m}) est couplée à une première entrée d'une unité de combinaison de signaux (46.1), une deuxième entrée de l'unité de combinaison de signaux étant couplée à une sortie d'une section à retard (44.1) de l'un des deux montages en série, une sortie de l'unité de combinaison de signaux étant couplée à une entrée de la section à retard suivante (44.2) dudit montage en série (40).

10. Système selon la revendication 4, 8 ou 9, caractérisé en ce que l'entrée (30) du filtre est couplée à la première et à la deuxième sorties via un premier et un deuxième trajets de signaux, respectivement, lesdits premier et deuxième trajets de signaux comprenant chacun une unité de multiplication (b_{pm}, c_{qm}) et étant connectés en parallèle au premier et au deuxième montages en série, respectivement.

11. Système selon la revendication 1 ou 2, caractérisé en ce que chaque filtre de synthèse comprend deux montages en série (52, 53) de sections à retard ayant un retard égal (2T), la première et la deuxième entrées (50.1, 50.2) du filtre étant couplées à une entrée de la première section à retard du premier et du deuxième montages en série, respectivement, des sorties d'au moins un certain nombre de sections à retard du premier montage en série étant couplées à des entrées correspondantes d'une unité de combinaison de signaux (54), des sorties d'au moins un certain nombre de sections à retard du deuxième montage en série étant également couplées à des entrées correspondantes de l'unité de combinaison de signaux, une sortie (60) de l'unité de combinaison de signaux étant couplée à la sortie (51) du filtre, une autre section à retard (55) ayant un retard (T) qui est égal à la moitié du retard des sections à retard des montages en série étant couplée dans le trajet des signaux de la deuxième entrée (50.2) à la sortie (51) du filtre, ladite autre section à retard n'étant pas incluse dans le trajet des signaux allant de la première entrée (50.1) à la sortie (51) du filtre.

12. Système selon la revendication 1 ou 2, caractérisé en ce que chaque filtre de synthèse comprend un montage en série (65) de sections à retard ayant un retard égal (T), la première entrée (50.2) du filtre étant couplée à des entrées d'au moins un certain nombre de sections à retard impaires (66.1, 66.3, ...) du montage en série, la deuxième entrée (50.1) du filtre étant couplée à des entrées d'au moins un certain nombre de sections à retard paires (66.2, 66.4, ...) du montage en série, la sortie de la dernière section à retard (66.n) étant couplée à la sortie (15) du filtre.

13. Système selon la revendication 12, caractérisé en ce que la première entrée du filtre est couplée à des entrées de sections à retard impaires seulement et la deuxième entrée du filtre est couplée à des entrées de sections à retard paires seulement.

14. Système selon la revendication 11, caractérisé en ce que les sorties des sections à retard du premier et du deuxième montages en série sont couplées à des entrées correspondantes de l'unité de combinaison de signaux via des unités de multiplication (d_{2m}, d_{3m}, e_{2m}, e_{3m}).

15. Système selon la revendication 11 ou 14, caractérisé en ce que la première et la deuxième entrées (50.2, 50.1) du filtre sont également couplées à des entrées correspondantes de l'unité de combinaison de signaux via des unités de multiplication (d_{1m}, e_{1m}).

16. Système selon la revendication 12 ou 13, caractérisé en ce que les entrées de filtre sont couplées aux entrées des sections à retard via des unités de multiplication (a_{1m}, a_{2m}, ...).

17. Système selon la revendication 16, caractérisé en ce qu'une sortie d'une unité de multiplication de signaux (67.3) est couplée à une première entrée d'une unité de combinaison de signaux, une deuxième entrée de l'unité de combinaison de signaux étant couplée à une sortie d'une section à retard (66.2) du montage en série, une sortie de l'unité de combinaison de signaux étant couplée à une entrée de la section à retard suivante (66.3) du montage en série.

18. Système selon la revendication 12, 13, 16 ou 17, caractérisé en ce que la deuxième entrée (50.2) du filtre est couplée à la sortie (51) du filtre via un trajet de signaux, ledit trajet de signaux comprenant une unité de multiplication (a_{0m}) et étant connecté en parallèle au montage en série.

19. Système selon la revendication 1 ou 2, caractérisé en ce que l'unité de traitement de signaux comprend M unités de combinaison de signaux (70.1, 70.2, ...), qui comporte une sortie couplée à une sortie correspondante (74.i) des M sorties de l'unité de traitement de signaux, et que pour chaque unité de combinaison de signaux, au moins un certain nombre d'entrées (71.1, 71.2, ...) des 2M entrées de l'unité de traitement est couplé à des entrées correspondantes de ladite unité de combinaison de signaux (70.1) via des unités de multiplication correspondantes (72.11, 72.12).

20. Système selon la revendication 1 ou 2, caractérisé en ce que l'autre unité de traitement de signaux correspondante comprend 2M unités de combinaison de signaux (70.1, 70.2, ...) qui comportent chacune une sortie couplée à une sortie correspondante des 2M sorties de l'unité de traitement et que pour chaque unité de combinaison de signaux (74.i), au moins un certain nombre d'entrées (71.1, 71.2, ...) des M entrées des unités de traitement est couplé à des entrées correspondantes de ladite unité de combinaison de signaux (70.1) via des unités de multiplication correspondantes (72.11, 72.12).

21. Système selon la revendication 1 ou 2, caractérisé en ce que les deux sorties de chaque filtre d'analyse sont chacune couplées à leurs entrées correspondantes de l'unité de traitement de signaux via une unité d'amplification de signaux correspondante (80.1, 81.1), les deux unités d'amplification étant à même d'amplifier les signaux appliqués à leurs entrées de la même valeur complexe (k_1).

22. Système selon la revendication 21, caractérisé en ce que les valeurs complexes (k_1, k_2, ...) sont différentes pour des unités d'amplification couplées à différents filtres d'analyse.

23. Système selon la revendication 21 ou 22, caractérisé en ce que chaque sortie (86.1) de l'unité de traitement est couplée à sa sortie correspondante (10.1) du codeur via un montage en série d'une unité d'amplification de signaux et d'un déterminateur de valeur réelle, l'unité d'amplification de signaux étant adaptée pour amplifier le signal appliqué à son entrée d'une valeur complexe.

24. Système selon la revendication 1 ou 2, caractérisé en ce que les deux sorties (93.1, 93.9) de chaque paire de sorties de l'autre unité de traitement de signaux (13′) sont chacune couplées à leur entrée correspondante d'un filtre de synthèse (16.1) via une unité d'amplification de signaux correspondante (94.1, 95.1), les deux unités d'amplification étant à même d'amplifier les signaux à leurs entrées de la même valeur complexe (k_1').

25. Système selon la revendication 24, caractérisé en ce que les valeurs complexes (k_1', k_2') sont différentes pour des unités d'amplification couplées à différents filtres de synthèse (16.1, 16.2,).

26. Système selon la revendication 1 ou 2, caractérisé en ce que les M entrées du décodeur sont couplées chacune à leur entrée correspondante des M entrées de l'autre unité de traitement via une unité d'amplification de signaux (90.1, 90.2, ...), l'unité d'amplification de signaux étant à même d'amplifier le signal appliqué à son entrée d'une autre valeur complexe (V_1', V_2', ...).

27. Système selon la revendication 23 ou 26, caractérisé en ce que les autres valeurs complexes sont différentes les unes des autres.

28. Système selon l'une quelconque des revendications 6 à 10 et 14 à 20, caractérisé en ce que les unités de multiplication pour lesquelles les facteurs de multiplication par lesquels elles multiplient leurs signaux d'entrée sont égaux à un, sont supprimées.

29. Système selon l'une quelconque des revendications 6 à 10 et 14 à 20, caractérisé en ce que les couplages qui comprennent une unité de multiplication pour laquelle le facteur de multiplication par lequel elle multiplie son signal d'entrée est égal à zéro, sont supprimés.

30. Système selon la revendication 1 ou 2, caractérisé en ce que l'unité de traitement de signaux (9″) comprend des moyens de commutation (100) et M unités de combinaison de signaux (102), chacune des 2M entrées (8.1 à 8.2M) de l'unité de traitement de signaux étant couplée à une entrée correspondante des 2M entrées des moyens de commutation, les moyens de commutation ayant une sortie (101) couplée à une entrée de chacune des M unités de combinaison de signaux (102), chaque unité de combinaison de signaux comprenant une unité de multiplication (106), une mémoire (107) ayant 2 M emplacements de stockage, un additionneur (108) et un registre de cumul (109), l'entrée de l'unité de combinaison de signaux et une sortie de la mémoire étant couplées à une première et une deuxième entrées (112, 111), respectivement, de l'unité de multiplication (106), une sortie de l'unité de multiplication et du registre de cumul (109) étant couplée à une première et à une deuxième entrées (113, 114), respectivement, de l'additionneur (108), l'additionneur ayant une sortie couplée à une entrée du registre, la sortie du registre (109) de la $m^{ème}$ unité de combinaison de signaux étant couplée à la $m^{ème}$ sortie (10.m) de l'unité de traitement de signaux (9″), les moyens de commutation (100) étant à même de coupler de manière cyclique chacune de ses 2M entrées (8.1 à 8.2M) à sa sortie (10.i) de manière à appliquer chaque fois les échantillons en des blocs de 2M échantillons qui se présentent à ses 2M entrées à raison d'un échantillon à chaque entrée, en série à sa sortie, la mémoire (107) comprenant 2M facteurs de multiplication (α), la mémoire étant à même de fournir de manière circulaire les 2M facteurs de multiplication à sa sortie, de telle sorte que le $i^{ème}$ facteur de multiplication soit délivré à sa sortie, lorsque les moyens de commutation (100) fournissent le $i^{ème}$ échantillon des 2M échantillons d'un bloc à sa sortie, où i est égal à 1 à 2M, l'additionneur (108) et le registre de cumul (109) étant à même d'ajouter le résultat de la $i^{ème}$ multiplication au contenu du registre de cumul, le registre de cumul étant, en outre, à même de délivrer son contenu obtenu après l'étape de la $2M^{ème}$ multiplication à la sortie (10.m) de l'unité de combinaison de signaux et de régler ensuite son contenu sur zéro.

31. Système selon la revendication 1 ou 2, caractérisé en ce que l'autre unité de traitement de signaux comprend des moyens de commutation (100) et 2M unités de combinaison de signaux (102), chacune des M entrées de l'autre unité de traitement de signaux étant couplée à une entrée correspondante des M entrées des moyens de commutation, les moyens de commutation ayant une sortie couplée à une entrée de chacune des 2M unités de combinaison de signaux, chaque unité de combinaison de signaux comprenant une unité de multiplication (106), une mémoire ayant M emplacements de stockage, un additionneur (108) et un registre de cumul (109), l'entrée de l'unité de combinaison de signaux et une sortie de la mémoire étant couplées à une première et une deuxième entrées, respectivement, de l'unité de multiplication (106), une sortie de l'unité de multiplication et du registre de cumul étant couplée à une première et une deuxième entrées, respectivement, de l'additionneur, l'additionneur ayant une sortie couplée à l'entrée du registre, la sortie du registre de la $i^{ème}$ unité de combinaison de signaux étant couplée à la $i^{ème}$ sortie de l'autre unité de traitement de signaux, où i est égal à 1 à 2M, le moyen de commutation étant à même de coupler de manière cyclique chacune de ses M entrées à sa sortie, de manière à appliquer, chaque fois des échantillons en blocs de M échantillons qui se présentent à ses M entrées, à raison d'un échantillon à chaque entrée, en série à sa sortie, la mémoire comprenant M facteurs de multiplication, la mémoire étant à même de fournir de manière circulaire les M facteurs de multiplication à sa sortie, de telle manière que le $m^{ème}$ facteur de multiplication soit délivré à sa sortie lorsque le moyen de commutation applique le $m^{ème}$ échantillon des M échantillons d'un bloc à sa sortie, l'additionneur et le registre de cumul étant à même d'ajouter le résultat de la $m^{ème}$ multiplication au contenu du registre de cumul, le registre de cumul étant, en outre, à même de délivrer son contenu obtenu après la $M^{ème}$ étape de multiplication à la sortie (101) de l'unité de combinaison de signaux et de régler son contenu à zéro ensuite.

32. Codeur pour codage en sous-bandes d'un signal numérique, tel qu'un signal audionumérique, ayant une cadence d'échantillonnage donnée F_s, le codeur étant sensible au signal numérique pour générer un nombre M de signaux de sous-bandes avec une réduction de la cadence d'échantillonnage, le codeur divisant la bande du signal numérique en sous-bandes successives de nombre de bandes m($1 \leqq m \leqq M$) augmentant avec la fréquence, le codeur (3, 6, 9) comprenant des moyens de filtrage par analyse (3, 6) et une unité de traitement de signaux (9), les moyens de filtrage par analyse comprennent M filtres d'analyse (6.1 à 6.M) ayant chacun une entrée et deux sorties, les 2M sorties des filtres étant couplées à 2M sorties des moyens de filtrage par analyse pour délivrer 2M signaux de sortie avec une cadence d'échan-

tillonnage F_s/M, chaque filtre d'analyse (6.1) étant à même d'appliquer deux filtrages différents au signal appliqué à son entrée (5.1) et de délivrer chacune des deux versions filtrées différentes de ce signal d'entrée à une sortie correspondante des deux sorties (7.1a, 7. 1b), chacune des 2M sorties des filtres étant couplée à une entrée correspondante de 2M entrées (8.1 à 8.2M) d'une unité de traitement de signaux (9), l'unité de traitement ayant M sorties (10.1 à 10.M) couplées à M sorties du codeur pour délivrer les M signaux de sous-bandes, l'unité de traitement de signaux étant à même de délivrer des signaux de sortie à chacune des M sorties, un signal de sortie étant une combinaison d'au moins un certain nombre de signaux d'entrée appliqués à ses 2M entrées, codeur dans lequel le codeur est à même de diviser la bande de signaux numériques en sous-bandes (B1, B2, ...) successives ayant des largeurs de bandes approximativement égales, caractérisé en ce que les coefficients de chacun des filtres d'analyse sont dérivés des coefficients d'un filtre standard (H(f)) ayant une caractéristique de filtrage passe-bas avec une largeur de bande approximativement égale à la moitié de la largeur des sous-bandes, que les coefficients des filtres d'analyse sont dérivés d'un filtre standard ayant un nombre impair de coefficients, que M est un nombre pair et, pour faire en sorte que le nombre de coefficients du filtre standard soit égal au nombre de facteurs de multiplication de chacun des filtres d'analyse, des zéros sont ajoutés à l'ensemble des coefficients du filtre standard.

33. Décodeur pour décoder M signaux de sous-bandes qui ont été obtenus par codage en sous-bandes d'un signal numérique en divisant la bande du signal numérique en largeurs de bande approximativement égales, le décodeur étant sensible aux M signaux de sous-bandes pour construire une réplique du signal numérique, ce décodeur fusionnant les sous-bandes en la bande de signal numérique avec une augmentation de la cadence d'échantillonnage, le décodeur (13, 16, 19) comprenant une unité de traitement de signaux (13) et des moyens de filtrage par synthèse (16, 19), l'unité de traitement de signaux ayant M entrées (12.1 à 12.M) pour recevoir les M signaux de sous-bandes et ayant 2M sorties (14.1 à 14.2M), les moyens de filtrage par synthèse comprenant M filtres de synthèse (16.1 à 16.M) comportant chacun deux entrées, et une sortie (20) couplée à la sortie du décodeur, l'autre unité de traitement de signaux (13) étant à même de générer un signal de sortie à chacune de ses 2M sorties, un signal de sortie étant une combinaison d'au moins un certain nombre de signaux d'entrée appliqués à ses M entrées, chaque paire de sorties (14.1, 14.2) de l'unité de traitement de signaux étant couplée à une paire de deux entrées (15.1a, 15.1b) d'un filtre correspondant des M filtres de synthèse (16.1 à 16.M), chaque filtre de synthèse (16.1) ayant une sortie (17.1), chaque filtre de synthèse étant à même d'appliquer différents filtrages sur les deux signaux appliqués aux deux entrées et de délivrer une combinaison des deux signaux filtrés à sa sortie, chaque sortie peut être couplée à la sortie des moyens de filtrage par synthèse pour délivrer la réplique du signal numérique ayant une cadence d'échantillonnage F_s, caractérisé en ce que les coefficients de chacun des filtres de synthèse sont dérivés des coefficients d'un filtre standard (H(f)) ayant une caractéristique de filtrage passe-bas avec une largeur de bande approximativement égale à la moitié de la largeur des sous-bandes, et que les coefficients pour les filtres de synthèse sont dérivés d'un filtre standard ayant un nombre impair de coefficients, que M est un nombre pair et que, pour faire en sorte que le nombre de coefficients du filtre standard soit égal au nombre de facteurs de multiplication de chacun des filtres de synthèse, des zéros sont ajoutés à l'ensemble des coefficients du filtre standard.

34. Emetteur pour émettre un signal numérique comprenant un codeur (3, 6, 9) pour codage en sous-bandes du signal numérique selon la revendication 32.

35. Récepteur pour recevoir un signal numérique qui a été codé à la transmission en un certain nombre de M signaux de sous-bandes en divisant la bande du signal numérique en sous-bandes de largeur de bande approximativement égale avec une réduction de la cadence d'échantillonnage, comprenant un décodeur selon la revendication 33.

36. Appareil d'enregistrement de signaux audionumériques pour enregistrer un signal audionumérique sur un support d'enregistrement, comprenant l'émetteur selon la revendication 34, caractérisé en ce qu'il comprend, en outre, des moyens d'enregistrement (120) comportant M entrées (121.1 à 121.M), chacune des M entrées étant couplée à une sortie correspondante des M sorties (10.1 à 10.M) de l'unité de traitement (9), les moyens d'enregistrement étant à même de transcrire les M signaux de sous-bandes appliqués à ses M entrées sur une piste du support d'enregistrement (122).

37. Appareil de reproduction de signaux audionumériques pour reproduire un signal audionumérique à partir d'un support d'enregistrement, comprenant le récepteur selon la revendication 35, caractérisé en ce qu'il

comprend, en outre, des moyens de reproduction (124) ayant M sorties (125.1 à 125.M), chacune des M sorties étant couplée à une entrée correspondante des M entrées (12.1 à 12.M) de l'unité de traitement (13), les moyens de reproduction étant à même de lire les M signaux de sous-bandes sur une piste du support d'enregistrement (122).

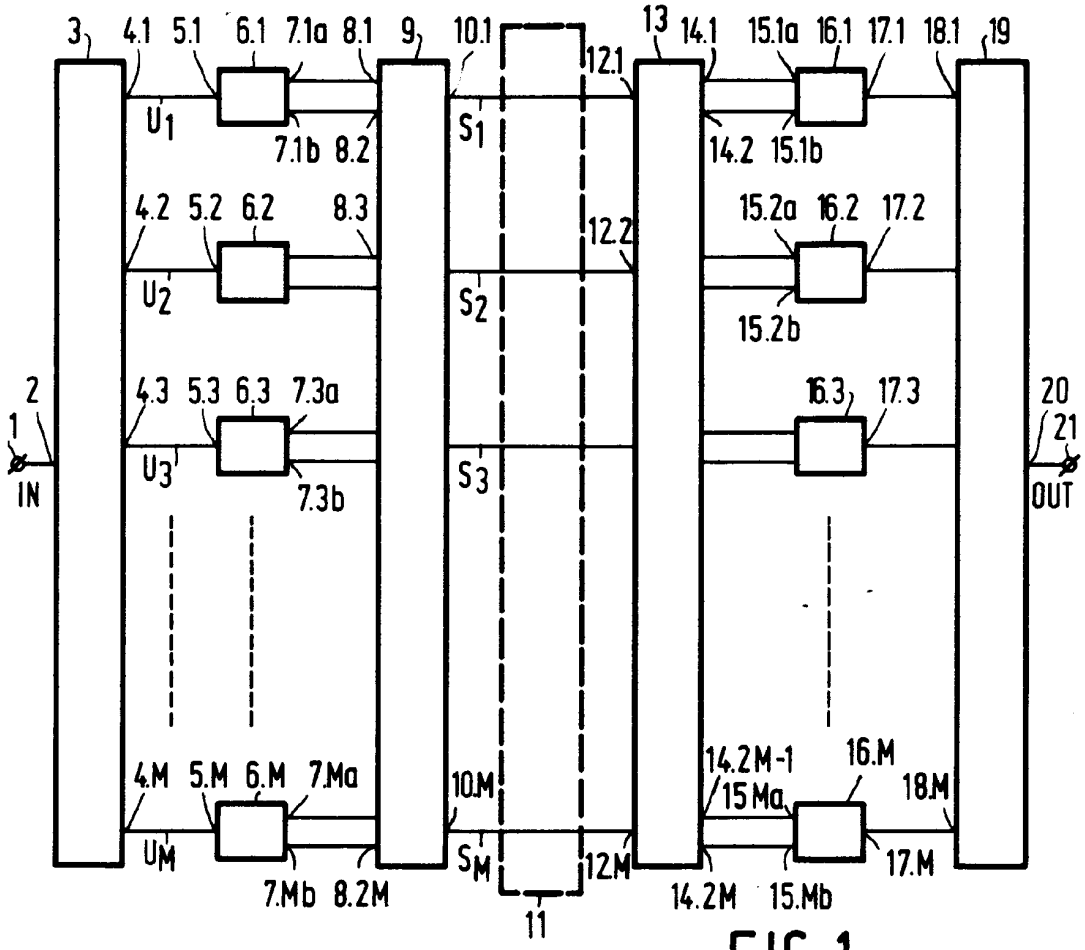

3
4.1
5.1
6.1
7.1a
8.1
9
10.1
12.1
13
14.1
15.1a
16.1
17.1
18.1
19
U1
7.1b
8.2
S1
14.2
15.1b
4.2
5.2
6.2
8.3
12.2
15.2a
16.2
17.2
U2
S2
15.2b
2
1
4.3
5.3
6.3
7.3a
16.3
17.3
20
21
IN
U3
7.3b
S3
OUT
4.M
5.M
6.M
7.Ma
10.M
14.2M-1
16.M
15Ma
18.M
UM
SM
12.M
7.Mb
8.2M
17.M
14.2M
15.Mb
11

FIG. 1

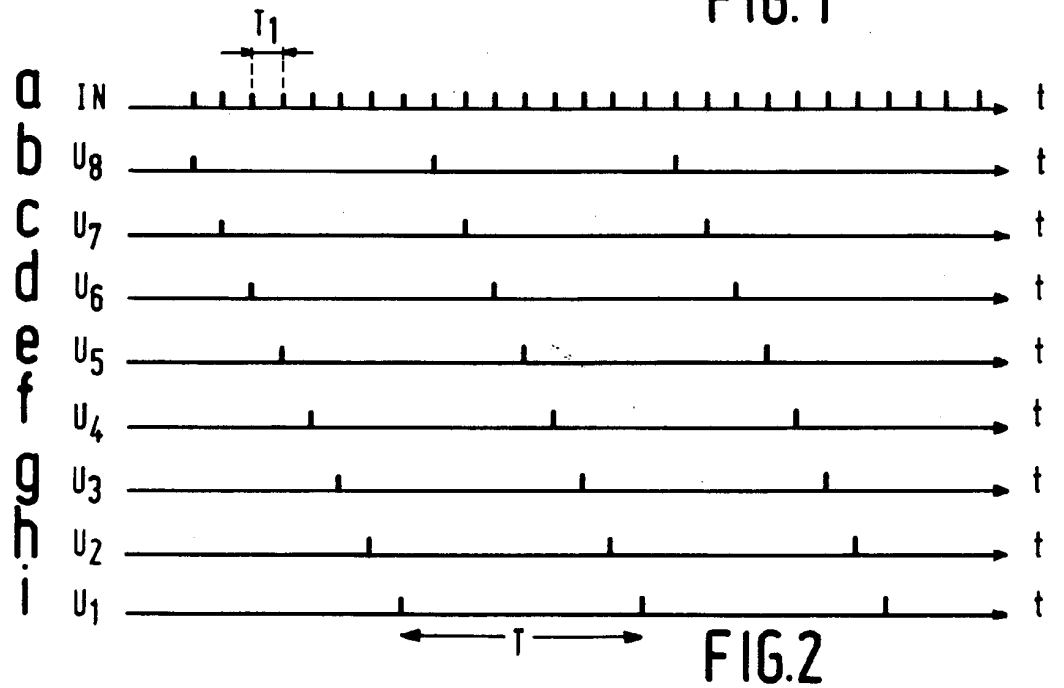

T1
a
IN
t
b
U8
c
U7
d
U6
e
U5
f
U4
g
U3
h
U2
i
U1
T

FIG. 2

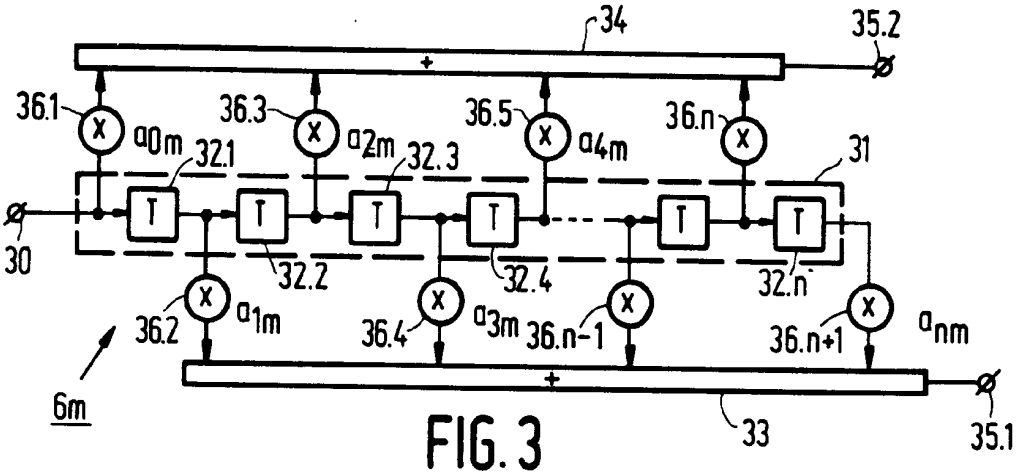


FIG. 3

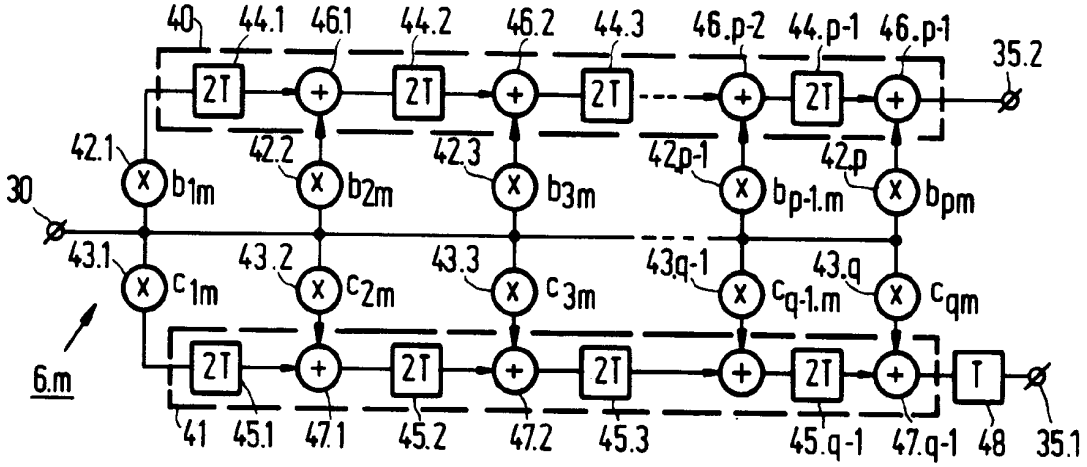


FIG. 4

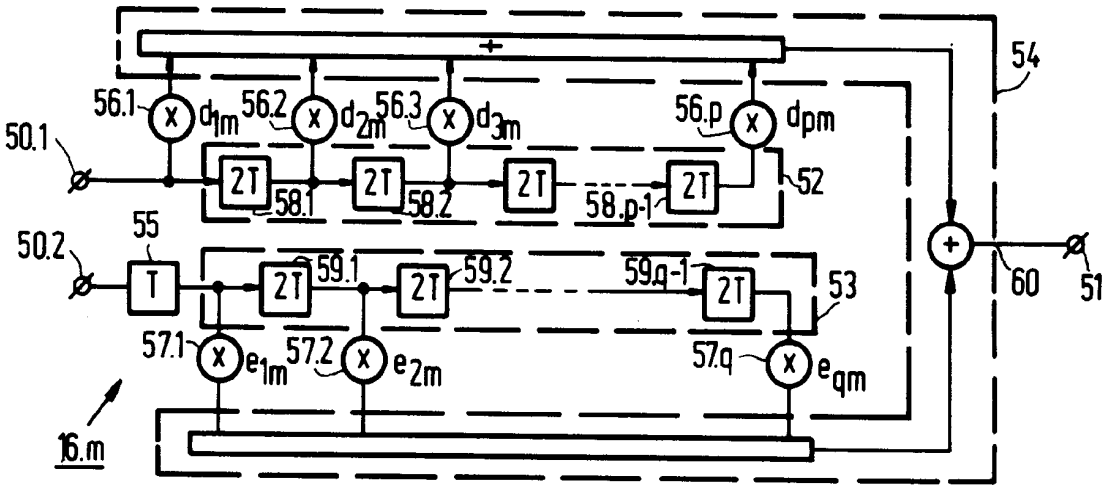


FIG. 5

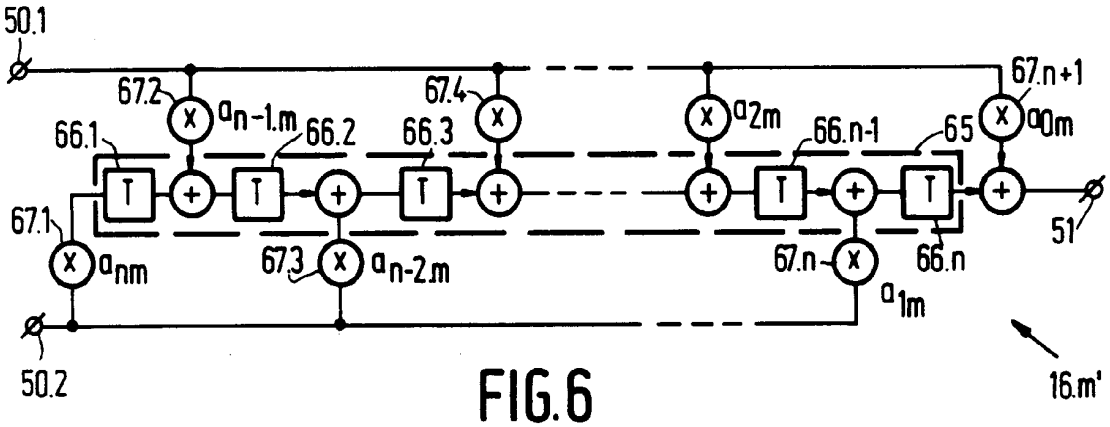

50.1
67.2
$a_{n-1,m}$
66.1
66.2
66.3
67.4
a_{2m}
66.n-1
65
67.n+1
a_{0m}
67.1
a_{nm}
67.3
$a_{n-2,m}$
67.n
a_{1m}
66.n
51
50.2
16.m'

FIG.6

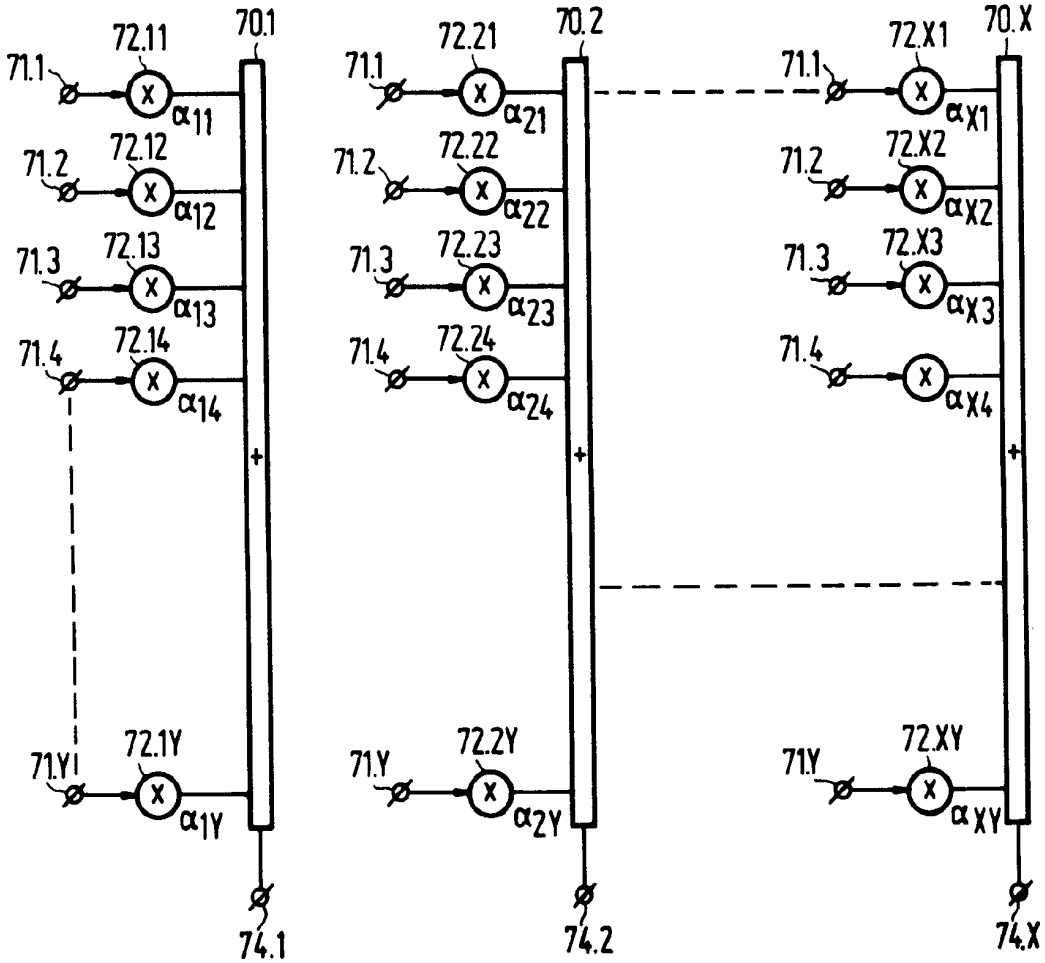

70.1
72.11
71.1
α_{11}
72.12
71.2
α_{12}
72.13
71.3
α_{13}
72.14
71.4
α_{14}
72.1Y
71.Y
α_{1Y}
74.1
70.2
72.21
71.1
α_{21}
72.22
71.2
α_{22}
72.23
71.3
α_{23}
72.24
71.4
α_{24}
72.2Y
71.Y
α_{2Y}
74.2
70.X
72.X1
71.1
α_{X1}
72.X2
71.2
α_{X2}
72.X3
71.3
α_{X3}
71.4
α_{X4}
72.XY
71.Y
α_{XY}
74.X

FIG.7

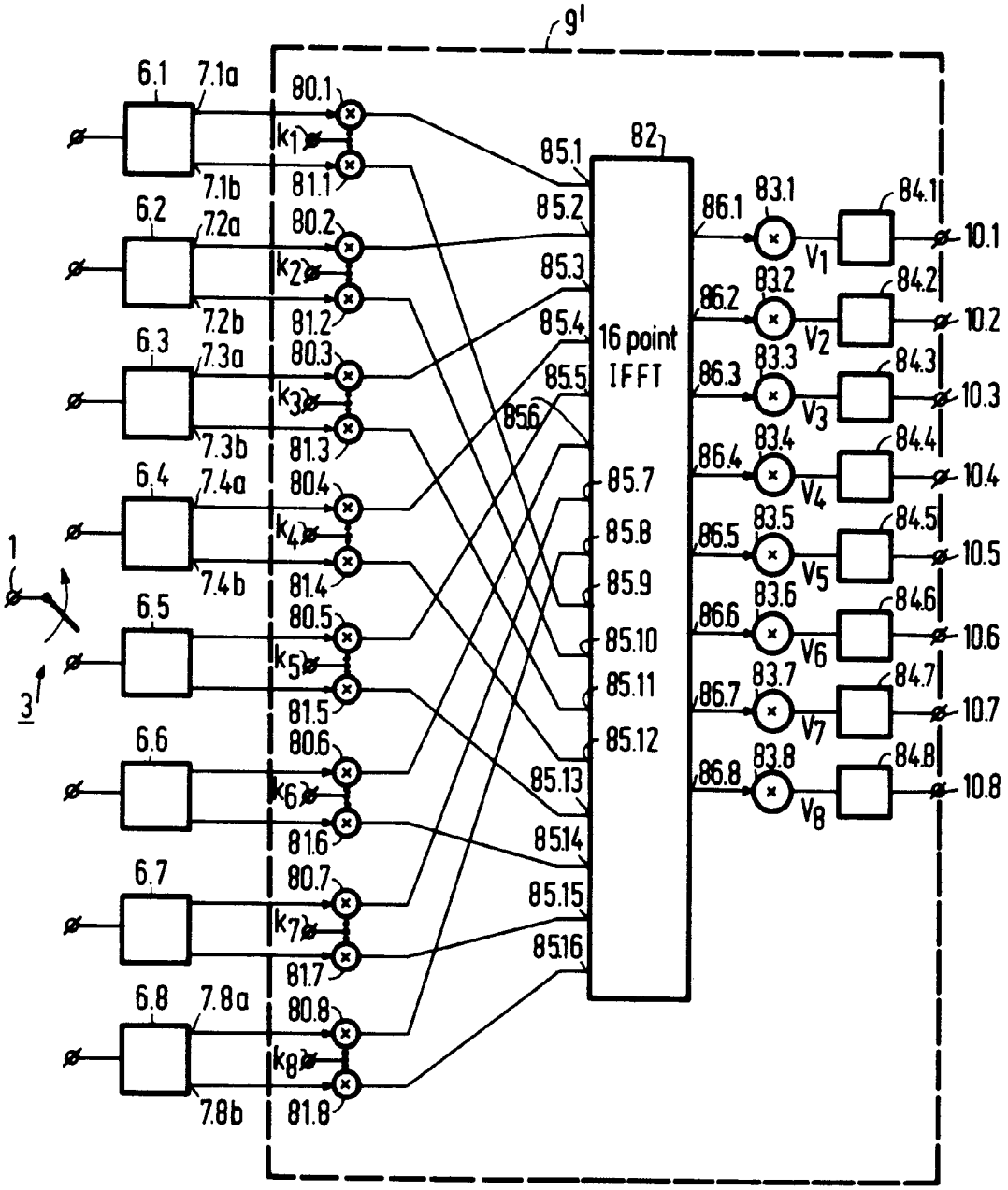
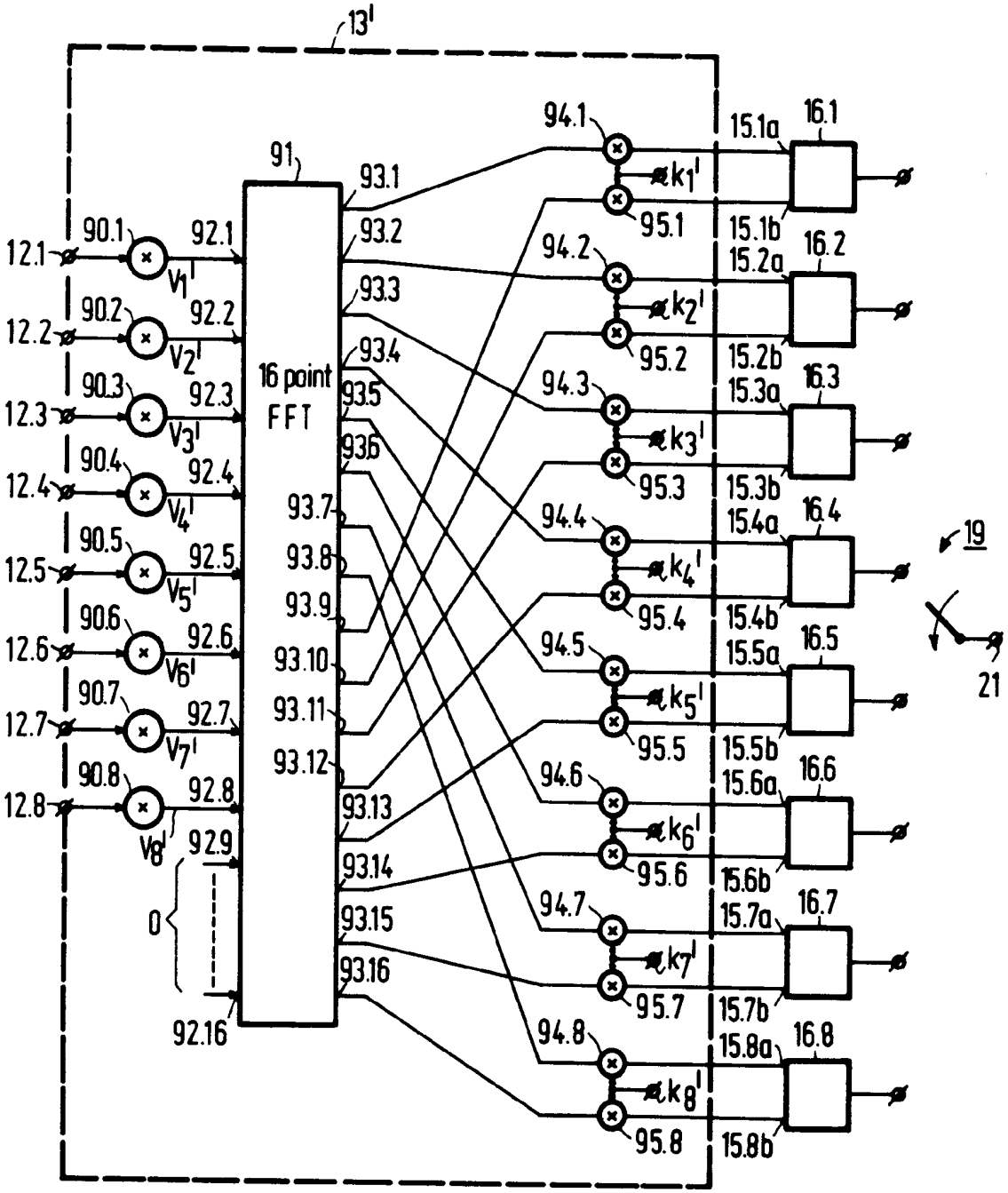

9'
6.1
7.1a
7.1b
6.2
7.2a
7.2b
6.3
7.3a
7.3b
6.4
7.4a
7.4b
6.5
6.6
6.7
6.8
7.8a
7.8b
1
3
80.1
80.2
80.3
80.4
80.5
80.6
80.7
80.8
k1
k2
k3
k4
k5
k6
k7
k8
81.1
81.2
81.3
81.4
81.5
81.6
81.7
81.8
85.1
85.2
85.3
85.4
85.5
85.6
85.7
85.8
85.9
85.10
85.11
85.12
85.13
85.14
85.15
85.16
82
16 point
IFFT
86.1
86.2
86.3
86.4
86.5
86.6
86.7
86.8
83.1
83.2
83.3
83.4
83.5
83.6
83.7
83.8
V1
V2
V3
V4
V5
V6
V7
V8
84.1
84.2
84.3
84.4
84.5
84.6
84.7
84.8
10.1
10.2
10.3
10.4
10.5
10.6
10.7
10.8

FIG.8


13'
91
16 point FFT
12.1
12.2
12.3
12.4
12.5
12.6
12.7
12.8
90.1
90.2
90.3
90.4
90.5
90.6
90.7
90.8
92.1
92.2
92.3
92.4
92.5
92.6
92.7
92.8
92.9
92.16
0
93.1
93.2
93.3
93.4
93.5
93.6
93.7
93.8
93.9
93.10
93.11
93.12
93.13
93.14
93.15
93.16
94.1
94.2
94.3
94.4
94.5
94.6
94.7
94.8
95.1
95.2
95.3
95.4
95.5
95.6
95.7
95.8
15.1a
15.1b
15.2a
15.2b
15.3a
15.3b
15.4a
15.4b
15.5a
15.5b
15.6a
15.6b
15.7a
15.7b
15.8a
15.8b
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16.2
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16.4
16.5
16.6
16.7
16.8
19
21

FIG.9

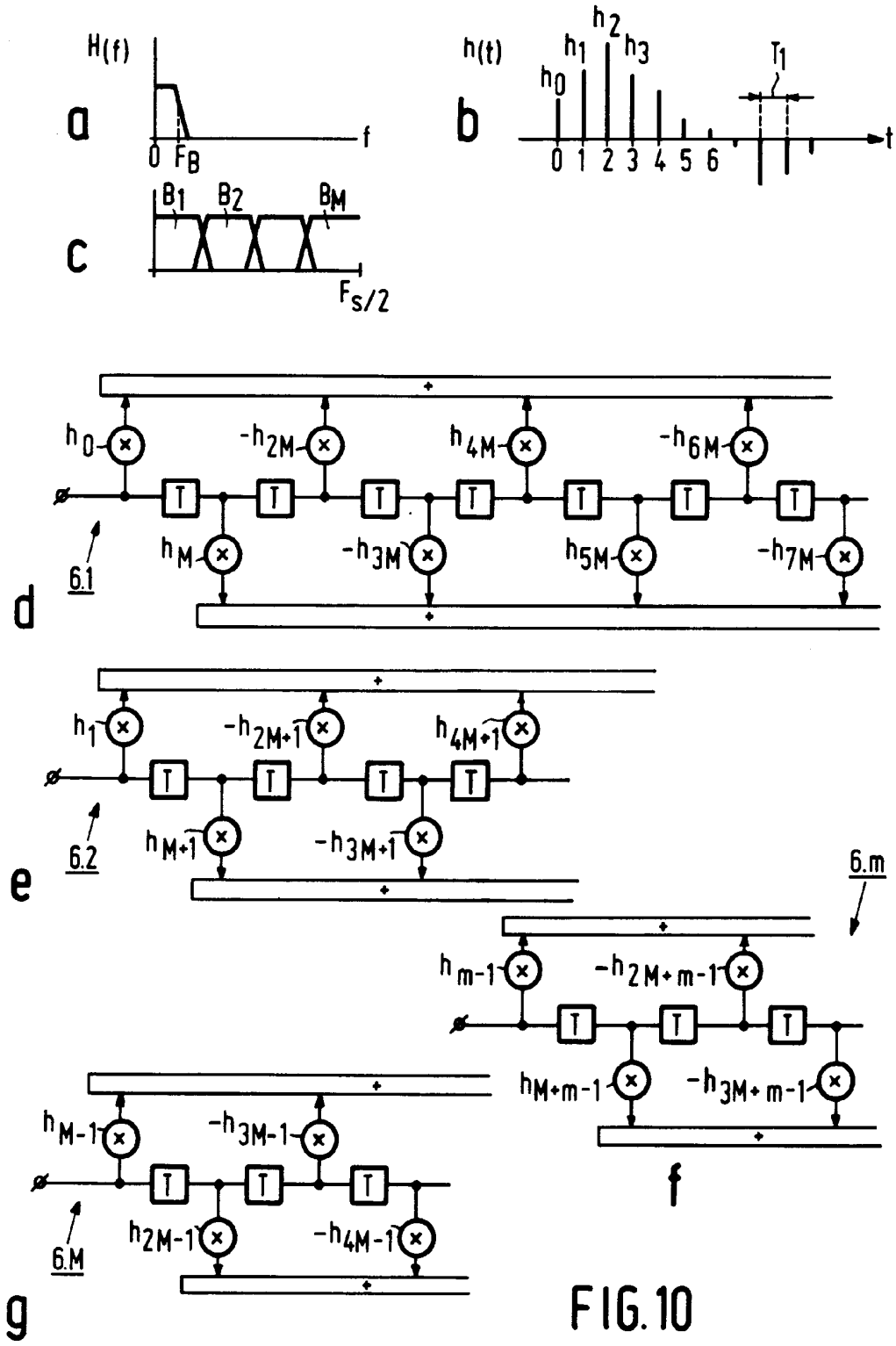
H(f)
a
0 FB
f
B1 B2 BM
c
Fs/2
h(t)
h0 h1 h2 h3
T1
b
0 1 2 3 4 5 6
t
h0 -h2M h4M -h6M
hM -h3M h5M -h7M
6.1
d
h1 -h2M+1 h4M+1
hM+1 -h3M+1
6.2
e
6.m
hm-1 -h2M+m-1
hM+m-1 -h3M+m-1
f
hM-1 -h3M-1
h2M-1 -h4M-1
6.M
g

FIG.10

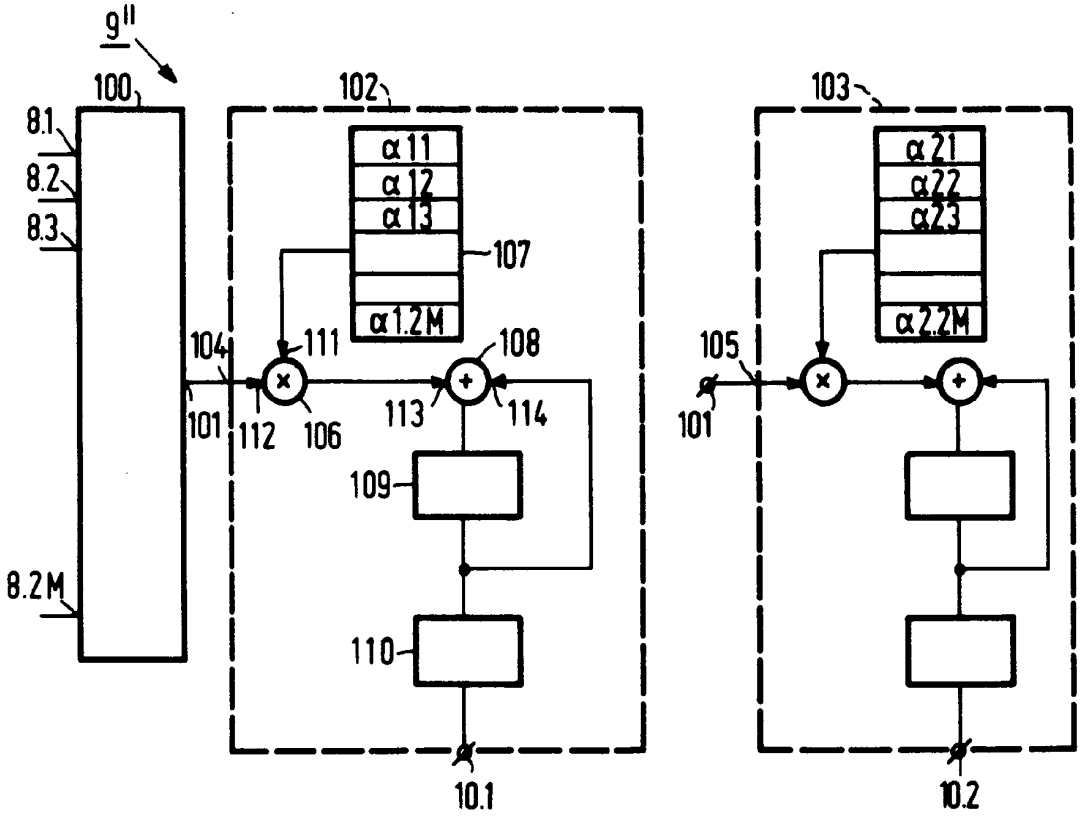
9''
100
102
103
8.1
8.2
8.3
8.2M
α11
α12
α13
α1.2M
107
α21
α22
α23
α2.2M
104
111
108
105
101
112
106
113
114
101
109
110
10.1
10.2

FIG. 11

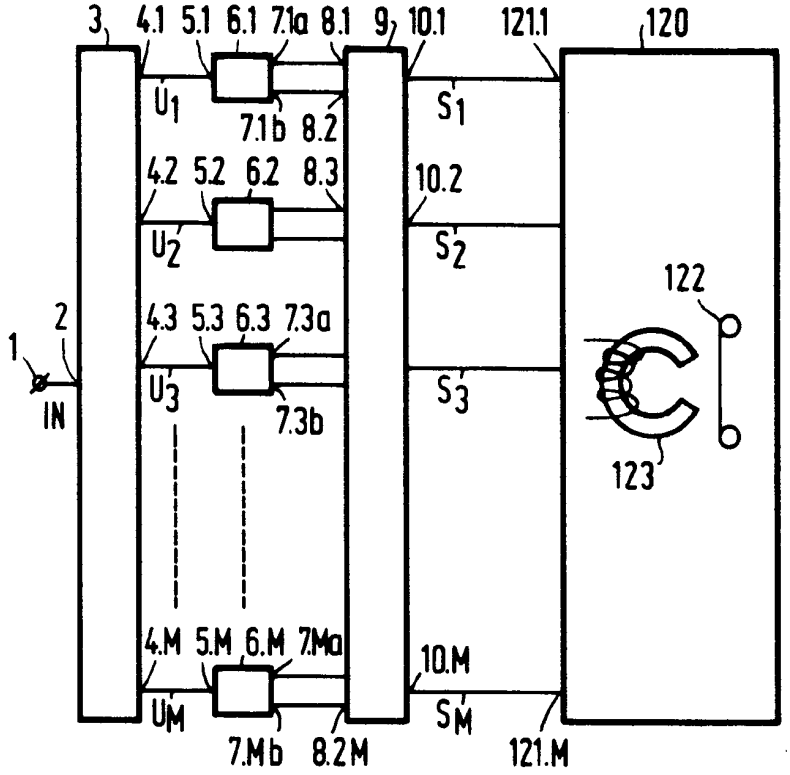
3
4.1
5.1
6.1
7.1a
8.1
9
10.1
121.1
120
U1
7.1b
8.2
S1
4.2
5.2
6.2
8.3
10.2
U2
S2
122
2
1
4.3
5.3
6.3
7.3a
IN
U3
7.3b
S3
123
4.M
5.M
6.M
7.Ma
10.M
UM
7.Mb
8.2M
SM
121.M

FIG. 12

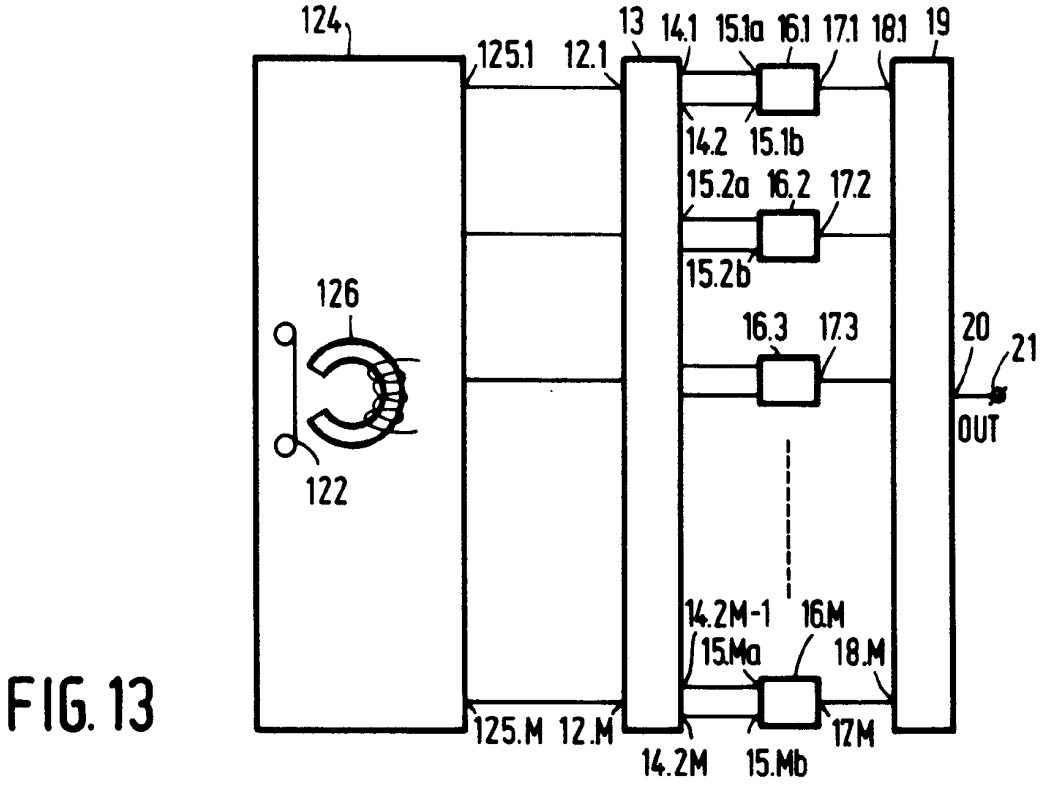
124
125.1
12.1
13
14.1
15.1a
16.1
17.1
18.1
19
14.2
15.1b
15.2a
16.2
17.2
15.2b
126
16.3
17.3
20
21
OUT
122
14.2M-1
16.M
15.Ma
18.M
125.M
12.M
17.M
14.2M
15.Mb

FIG. 13

α_{xy}

x =	y = 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	0.707107	0.707107	0.831470	0.555570	0.923880	0.382683	0.980785	0.195090	1.000000	0.000000	0.980785	-0.195090	0.923880	-0.382683	0.831470	-0.555570
2	-0.707107	-0.707107	-0.195090	-0.980785	0.382683	-0.923880	0.831470	-0.555570	1.000000	0.000000	0.831470	0.555570	0.382683	0.923880	-0.195090	0.980785
3	-0.707107	-0.707107	-0.980785	0.195090	-0.382683	0.923880	0.555570	0.831470	1.000000	0.000000	0.555570	-0.831470	-0.382683	-0.923880	-0.980785	-0.195090
4	0.707107	0.707107	-0.555570	0.831470	-0.923880	-0.382683	0.195090	-0.980785	1.000000	0.000000	0.195090	0.980785	-0.923880	0.382683	-0.555570	-0.831470
5	0.707107	0.707107	0.555570	-0.831470	-0.923880	-0.382683	-0.195090	0.980785	1.000000	0.000000	-0.195090	-0.980785	-0.923880	0.382683	0.555570	0.831470
6	-0.707107	-0.707107	0.980785	-0.195090	-0.382683	0.923880	-0.555570	-0.831470	1.000000	0.000000	-0.555570	0.831470	-0.382683	-0.923880	0.980785	0.195090
7	-0.707107	-0.707107	0.195090	0.980785	0.382683	-0.923880	-0.831470	0.555570	1.000000	0.000000	-0.831470	-0.555570	0.382683	0.923880	0.195090	-0.980785
8	0.707107	0.707107	-0.831470	-0.555570	0.923880	0.382683	-0.980785	-0.195090	1.000000	0.000000	-0.980785	0.195090	0.923880	-0.382683	-0.831470	0.555570

Tab. I

α_{xy}

x=	y = 1	2	3	4	5	6	7	8
1	0.707107	-0.707107	-0.707107	0.707107	0.707107	-0.707107	-0.707107	0.707107
2	-0.707107	0.707107	0.707107	-0.707107	-0.707107	0.707107	0.707107	-0.707107
3	0.555570	-0.980785	0.195090	0.831470	-0.831470	-0.195090	0,980785	-0.555570
4	-0.831470	0.195090	0.980785	0.555570	-0.555570	-0.980785	-0.195090	0.831470
5	0.382683	-0.923880	0.923880	-0.382683	-0.382683	0.923880	-0.923880	0.382683
6	-0.923880	-0.382683	0.382683	0.923880	0.923880	0.382683	-0.382683	-0.923880
7	0.195090	-0.555570	0.831470	-0.980785	0.980785	-0.831470	0.555570	-0.195090
8	-0.980785	-0.831470	-0.555570	-0.195090	0.195090	0.555570	0.831470	0.980785
9	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000
10	-1.000000	-1.000000	-1.000000	-1.000000	-1.000000	-1.000000	-1.000000	-1.000000
11	-0.195090	0.555570	-0.831470	0.980785	-0.980785	0.831470	-0.555570	0.195090
12	-0.980785	-0.831470	-0.555570	-0.195090	0.195090	0.555570	0.831470	0.980785
13	-0.382683	0.923880	-0.923880	0.382683	0.382683	-0.923880	0.923880	-0.382683
14	-0.923880	-0.382683	0.382683	0.923880	0.923880	0.382683	-0.382683	-0.923880
15	-0.555570	0.980785	-0.195090	-0.831470	0.831470	0.195090	-0.980785	0.555570
16	-0.831470	0.195090	0.980785	0.555570	-0.555570	-0.980785	-0.195090	0.831470

Tab. II

	m = 1	m = 2	m = 3	m = 4
α_{0m}	0.0000000000000E+000	-1.125743279792E-006	-2.309778870789E-006	-4.375300768003E-006
	-5.651056006465E-005	-8.365624375053E-005	-1.191716111159E-004	-1.634573198230E-004
	4.4097771833693E-004	4.6676278790530E-004	4.5955626817648E-004	4.0639344025097E-004
	-9.287922047996E-004	-1.429998555824E-003	-1.982683016328E-003	-2.555984489389E-003
	3.9706288624499E-003	3.5326231891154E-003	2.7192140468306E-003	1.4962891295696E-003
	-1.002667672173E-002	-1.277770232641E-002	-1.529566154027E-002	-1.735583793213E-002
	1.2505823684771E-002	7.1149249057260E-003	-2.373922354461E-006	-8.818440634321E-003
	-7.165157960042E-002	-8.558941585606E-002	-9.895032702828E-002	-1.112550048227E-001
	1.4294960225719E-001	1.4157586813574E-001	1.3750965670085E-001	1.3091303152516E-001
	7.1651579600422E-002	5.7615021392889E-002	4.3934320358719E-002	3.1020230584892E-002
	1.2505823684771E-002	1.6219484317021E-002	1.8372138633404E-002	1.9134465393578E-002
	1.0026676721731E-002	7.2412214206719E-003	4.5869394188187E-003	2.1922350584038E-003
	3.9706288624499E-003	4.0841947050998E-003	3.9346487797243E-003	3.5877078759142E-003
	9.2879220479961E-004	4.9928534433306E-004	1.5193148310472E-004	-1.111018284468E-004
	4.4097771833698E-004	3.9402151065032E-004	3.3594819066619E-004	2.7467345877845E-004
α_{nm}	5.6510560064671E-005	3.6699481591696E-005	2.2903822447726E-005	1.3729632747217E-005

	m = 5	m = 6	m = 7	m = 8
α_{0m}	-7.911603287751E-006	-1.372963274719E-005	-2.290382244771E-005	-3.669948159168E-005
	-2.159455868186E-004	-2.746734587784E-004	-3.359481906661E-004	-3.940215106503E-004
	2.9420158901097E-004	1.1110182844680E-004	-1.519314831047E-004	-4.992853443330E-004
	-3.108217659565E-003	-3.587707875914E-003	-3.934648779724E-003	-4.084194705100E-003
	-1.469947276883E-004	-2.192235058404E-003	-4.586939418819E-003	-7.241221420672E-003
	-1.871719572738E-002	-1.913446539358E-002	-1.837213863340E-002	-1.621948431702E-002
	-1.922275084523E-002	-3.102023058489E-002	-4.393432035872E-002	-5.761502139289E-002
	-1.220464497130E-001	-1.309130315252E-001	-1.375096567009E-001	-1.415758681357E-001
	1.2204644971303E-001	1.1125500482267E-001	9.8950327028276E-002	8.5589415856063E-002
	1.9222750845235E-002	8.8184406343208E-003	2.3739223544652E-006	-7.114924905726E-003
	1.8717195727383E-002	1.7355837932130E-002	1.5295661540271E-002	1.2777702326405E-002
	1.4699472768831E-004	-1.496289129570E-003	-2.719214046831E-003	-3.532623189115E-003
	3.1082176595649E-003	2.5559844893895E-003	1.9826830163279E-003	1.4299985558238E-003
	-2.942015890110E-004	-4.063934402510E-004	-4.595562681765E-004	-4.667627879054E-004
	2.1594558681868E-004	1.6345731982306E-004	1.1917161111588E-004	8.3656243750563E-005
α_{nm}	7.9116032877609E-006	4.3753007680050E-006	2.3097788707847E-006	1.1257432798081E-006

Tab. III

α_{xy}

x =	y = 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	0.634393	-0.773010	0.471397	-0.881921	0.290285	-0.956940	0.098017	-0.995185	-0.098017	-0.995185	-0.290285	-0.956940	-0.471397	-0.881921	-0.634393	-0.773010
2	0.881921	-0.471397	0.995185	0.098017	0.773010	0.634393	0.290285	0.956940	-0.290285	0.956940	-0.773010	0.634393	-0.995185	0.098017	-0.881921	-0.471397
3	0.290285	-0.956940	-0.634393	-0.773010	-0.995185	0.098017	-0.471397	0.881921	0.471397	0.881921	0.995185	0.098017	0.634393	-0.773010	-0.290285	-0.956940
4	0.995185	-0.098017	0.290285	0.956940	-0.881921	0.471397	-0.634393	-0.773010	0.634393	-0.773010	0.881921	0.471397	-0.290285	0.956940	-0.995185	-0.098017
5	-0.098017	-0.995185	-0.956940	0.290285	0.471397	0.881921	0.773010	-0.634393	-0.773010	-0.634393	-0.471397	0.881921	0.956940	0.290285	0.098017	-0.995185
6	0.956940	0.290285	-0.773010	0.634393	-0.098017	-0.995185	0.881921	0.471397	-0.881921	0.471397	0.098017	-0.995185	0.773010	0.634393	-0.956940	0.290285
7	-0.471397	-0.881921	-0.098017	0.995185	0.634393	-0.773010	-0.956940	0.290285	0.956940	0.290285	-0.634393	-0.773010	0.098017	0.995185	0.471397	-0.881921
8	0.773010	0.634393	-0.881921	-0.471397	0.956940	0.290285	-0.995185	-0.098017	0.995185	-0.098017	-0.956940	0.290285	0.881921	-0.471397	-0.773010	0.634393

Tab. IV

α_{xy}

x =	y = 1	2	3	4	5	6	7	8
1	0.773010	0.471397	0.956940	0.098017	0.995185	-0.290285	0.881921	-0.634393
2	0.634393	0.881921	0.290285	0.995185	-0.098017	0.956940	-0.471397	0.773010
3	0.881921	-0.098017	0.773010	-0.956940	-0.290285	-0.634393	-0.995185	0.471397
4	0.471397	0.995185	-0.634393	0.290285	-0.956940	-0.773010	-0.098017	-0.881921
5	0.956940	-0.634393	-0.098017	-0.471397	-0.881921	0.995185	0.773010	-0.290285
6	0.290285	0.773010	-0.995185	-0.881921	0.471397	-0.098017	0.634393	0.956940
7	0.995185	-0.956940	-0.881921	0.773010	0.634393	-0.471397	-0.290285	0.098017
8	0.098017	0.290285	-0.471397	-0.634393	0.773010	0.881921	-0.956940	-0.995185
9	0.995185	-0.956940	-0.881921	0.773010	0.634393	-0.471397	-0.290285	0.098017
10	-0.098017	-0.290285	0.471397	0.634393	-0.773010	-0.881921	0.956940	0.995185
11	0.956940	-0.634393	-0.098017	-0.471397	-0.881921	0.995185	0.773010	-0.290285
12	-0.290285	-0.773010	0.995185	0.881921	-0.471397	0.098017	-0.634393	-0.956940
13	0.881921	-0.098017	0.773010	-0.956940	-0.290285	-0.634393	-0.995185	0.471397
14	-0.471397	-0.995185	0.634393	-0.290285	0.956940	0.773010	0.098017	0.881921
15	0.773010	0.471397	0.956940	0.098017	0.995185	-0.290285	0.881921	-0.634393
16	-0.634393	-0.881921	-0.290285	-0.995185	0.098017	-0.956940	0.471397	-0.773010

Tab. V

	m=1	m=2	m=3	m=4
α_{0m}	-0.000006864	-0.000012066	-0.000017945	-0.000023822
	-0.000027413	-0.000021448	-0.000015149	-0.000010485
	0.000076330	0.000106429	0.000132695	0.000145907
	-0.000411472	-0.000718016	-0.001091056	-0.001513963
	0.002985591	0.002743399	0.002173260	0.001226473
	-0.009015025	-0.011620369	-0.014037416	-0.016032039
	0.010718051	0.005059027	-0.002417056	-0.011679944
	-0.077205460	-0.091476873	-0.104986604	-0.117212139
	0.144530152	0.141616726	0.135914256	0.127664368
	0.062700586	0.048469218	0.034972535	0.022605254
	0.014616596	0.016886280	0.017718595	0.017347635
	0.006422689	0.004004989	0.001880537	0.000124915
	0.002961552	0.002738731	0.002383966	0.001958420
	0.000177740	0.000014811	-0.000085354	-0.000134492
	0.000048905	0.000027980	0.000015035	0.000009722
α_{nm}	0.000031619	0.000033287	0.000032255	0.000028872

	m=5	m=6	m=7	m=8
α_{0m}	-0.000028872	-0.000032255	-0.000033287	-0.000031619
	-0.000009722	-0.000015035	-0.000027980	-0.000048905
	0.000134492	0.000085354	-0.000014811	-0.000177740
	-0.001958420	-0.002383966	-0.002738731	-0.002961552
	-0.000124915	-0.001880537	-0.004004989	-0.006422689
	-0.017347635	-0.017718595	-0.016886280	-0.014616596
	-0.022605254	-0.034972535	-0.048469218	-0.062700586
	-0.127664368	-0.135914256	-0.141616726	-0.144530152
	0.117212139	0.104986604	0.091476873	0.077205460
	0.011679944	0.002417056	-0.005059027	-0.010718051
	0.016032039	0.014037416	0.011620369	0.009015025
	-0.001226473	-0.002173260	-0.002743399	-0.002985591
	0.001513963	0.001091056	0.000718016	0.000411472
	-0.000145907	-0.000132695	-0.000106429	-0.000076330
	0.000010485	0.000015149	0.000021448	0.000027413
α_{nm}	0.000023822	0.000017945	0.000012066	0.000006864

Tab. VI